MAX9286 Programming Guide

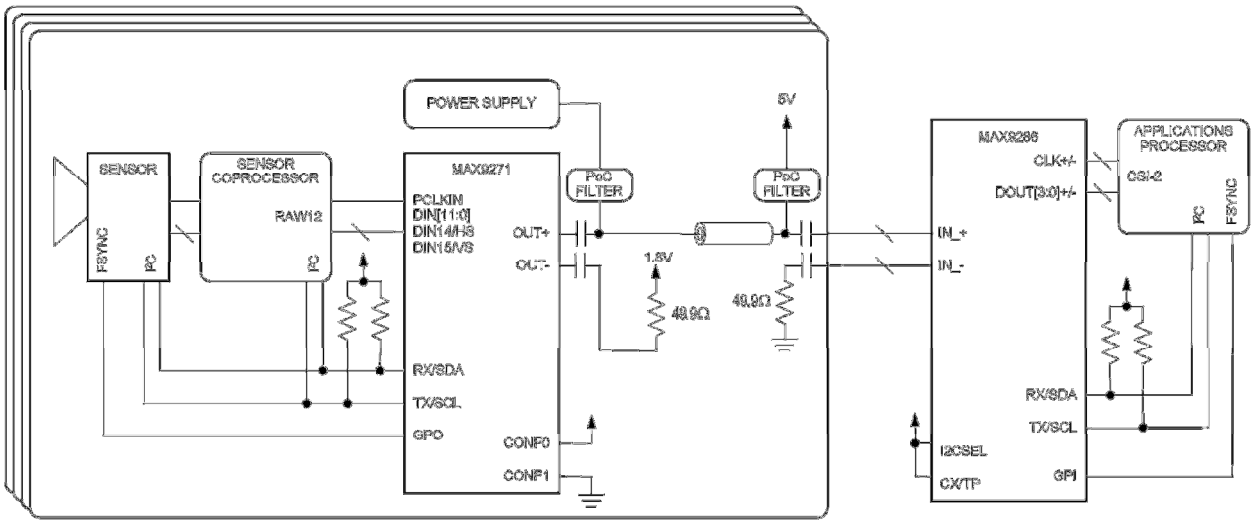
Abstract: This document provides general setup procedures for the MAX9286 Quad Gigabit Multimedia Serial Link (GMSL) Deserializer.

Introduction

The MAX9286 GMSL deserializer receives data from up to 4 GMSL serializers over 50Ω coax or 100Ω shielded twisted pair (STP) cables. The combined image data is output via CSI-2. Automatic frame synchronization allows the MAX9286 to align up to 4 image sensors. Programming can be divided into 6 parts, each of will be dealt with separately.

1. **Reverse Channel Setup**
2. **MAX9286 Initial Setup**
3. **GMSL Link Setup**
4. **Image Sensor Initialization**
5. **Enable GMSL & CSI-2**
6. **Verification**

Figure: Typical Application Circuit



Setup Sequence Example for MAX9286, Four MAX9271, RAW8x2

Note: if using other data types, Set the DATATYPE bits (register 0x12) accordingly. See the MAX9286 datasheet for details.

1. *Reverse Channel Setup*

It is important to establish a robust I2C connection between the deserializer and serializer. With the addition of power over coax, four serial links, and an inherently noisy environment; default reverse channel settings will need to be adjusted. After power up it is important to adjust the deserializer's amplitude and the serializer's input levels before any other I2C transactions to avoid unwanted effects on the serializers I2C registers.

Table: Reverse Channel Setup Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
1	Write	DES	0x90	0x3F	0x4F	Enable Custom Reverse Channel & First Pulse Length
2	Delay				2ms	Wait 2ms after any change to reverse channel settings *Note 2
3	Write	DES	0x90	0x3B	0x1E	First pulse length rise time changed from 300ns to 200ns
4	Delay				2ms	Wait 2ms after any change to reverse channel settings *Note 2
5	Write	SER	0x80	0x04	0x43	Optional - Enable configuration link *Note 1
6	Delay				5ms	Wait 5ms for configuration link to establish
7	Write	SER	0x80	0x08	0x01	Enable high threshold for reverse channel input buffer. This increases immunity to power supply noise when the coaxial link is used for power as well as signal.
8	Delay				2ms	Wait 2ms after any change to reverse channel settings *Note 2
9	Write	DES	0x90	0x3B	0x19	Increase reverse amplitude from 100mV to 170mV. This compensates for the higher threshold of step 5.

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
10	Delay				2ms	Wait 2ms after any change to reverse channel settings *Note 2

***Note 1:** Lines 5 & 6 are only needed after powerup or for Acknowledge or I2C read back from the serializer when there is no PCLK to establish the forward link. Line 5 will enable configuration link on all devices with the slave address 0x80. Therefore verification of initial I2C robustness settings should be performed with a single link or the slave addresses made unique for each serializer. Section 3 – 6 address how to change each serializers slave address and create a broadcast address once changed.

***Note 2:** 2ms of delay is needed after any analog change to the reverse channel for bus timeout and for the I2C state machine to settle from any glitches.

***Note 3:** The control channel cannot be used while establishing a link, 5ms of delay is required to establish the configuration link.

2. MAX9286 Initial Setup

After reverse channel settings the CSI-2 output can be disabled until frame sync is achieved. Register 0x12 selects the CSI lanes, CSI & GMSL Double Mode and the video data type. MAX9286 DBL=0 for RAWx1 or DBL=1 or RAWx2 / YUV 422. CSI-2 DBL is the users preference based on system requirements or by data rate.

Table: MAX9286 Initial Setup Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
11	Write	DES	0x90	0x15	0x03	Disable CSI output
12	Write	DES	0x90	0x12	0xF5	Enable CSI-2 Lanes D0, D1, D2, D3 Enable CSI-2 DBL Enable GMSL DBL for RAWx2 Enable RAW 8 data type
13	Write	DES	0x90	0x01	0x01	Enable frame sync Enable semi-auto frame sync. Use semi-auto for row reset on frame sync sensors Use auto for row/column reset on frame sync sensors
14	Write	DES	0x90	0x00	0xEF	Force master link or select auto. First GMSL link to lock will be mater link with auto select Disable internal VSYNC generation. Use free running VSYNC from image sensor Enable GMSL links

3. GMSL Link Setup

Each serializer needs to be setup individually and their respective I2C slave address changed to a unique value. Because the MAX9286 has quad GMSL inputs all the MAX9271's will power up with the same slave address. To combat this enable one reverse channel (REVCCEN_) at a time via register 0x0A in MAX9286 and change the MAX9271 slave address in register 0x00. If the image sensors have the same slave address the I2C translation registers 0x09 & 0x0A can be utilized to create a unique I2C slave address. The same approach can be applied to create a MAX9271 broadcast slave address. Simply write the broadcast address to register 0x0B and the respective MAX9271 address to register 0x0C. (see the table below)

Table: Example MAX9271 Address Translation Register Settings

MAX9271	REG 0X00	REG 0x09	REG 0x0A	REG 0x0B	REG 0x0C
Link 0	0x82	0x62	0x60	0x8A	0x82
Link 1	0x84	0x64	0x60	0x8A	0x84
Link 2	0x86	0x66	0x60	0x8A	0x86
Link 3	0x88	0x68	0x60	0x8A	0x88

Note: Keep the default serializer address 0x80 reserved to allow easy detection and initialization in case of a Power-on-reset in one of the camera modules

Table: GMSL Link Setup Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
15	Write	DES	0x90	0x0A	0xF1	Enable Link 0 Reverse Channel
16	Write	SER	0x80	0x00	0x82	Change serializer slave address
17	Write	SER	0x82	0x07	0x94	Enable DBL Set Edge Select 1=Rise / 0=Fall Enable HS/VS encoding
18	Write	SER	0x82	0x09	0x62	Unique Link 0 image sensor slave address
19	Write	SER	0x82	0x0A	0x60	Link 0 image sensor slave address
20	Write	SER	0x82	0x0B	0x8A	Serializer broadcast address

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
21	Write	SER	0x82	0x0C	0x82	Link 0 serializer address
22	Write	DES	0x90	0x0A	0xF2	Enable Link 1 Reverse Channel
23	Write	SER	0x80	0x00	0x84	Change serializer slave address
24	Write	SER	0x84	0x07	0x94	Enable DBL Set Edge Select 1=Rise / 0=Fall Enable HS/VS encoding
25	Write	SER	0x84	0x09	0x64	Unique Link 1 image sensor slave address
26	Write	SER	0x84	0x0A	0x60	Link 1 image sensor slave address
27	Write	SER	0x84	0x0B	0x8A	Serializer broadcast address
28	Write	SER	0x84	0x0C	0x84	Link 1 serializer address
29	Write	DES	0x90	0x0A	0xF4	Enable Link 2 Reverse Channel
30	Write	SER	0x80	0x00	0x86	Change serializer slave address
31	Write	SER	0x86	0x07	0x94	Enable DBL Set Edge Select 1=Rise / 0=Fall Enable HS/VS encoding
32	Write	SER	0x86	0x09	0x66	Unique Link 2 image sensor slave address
33	Write	SER	0x86	0x0A	0x60	Link 2 image sensor slave address
34	Write	SER	0x86	0x0B	0x8A	Serializer broadcast address
35	Write	SER	0x86	0x0C	0x86	Link 2 serializer address
36	Write	DES	0x90	0x0A	0xF8	Enable Link 3 Reverse Channel
37	Write	SER	0x80	0x00	0x88	Change serializer slave address

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
38	Write	SER	0x88	0x07	0x94	Enable DBL Set Edge Select 1=Rise / 0=Fall Enable HS/VS encoding
39	Write	SER	0x88	0x09	0x68	Unique Link 3 image sensor slave address
40	Write	SER	0x88	0x0A	0x60	Link 3 image sensor slave address
41	Write	SER	0x88	0x0B	0x8A	Serializer broadcast address
42	Write	SER	0x88	0x0C	0x88	Link 3 serializer address
44	Write	DES	0x90	0x0A	0xFF	Enable all I2C reverse channels

4. Image Sensor Initialization

Two feedback approaches can be taken when initializing the image sensor. Read back after each write or utilize I2C acknowledge. Both will require the configuration link to be enabled in step 9. For I2C acknowledge method disable auto ACK in register 0x34 of MAX9286.

Table: Image Sensor Initialization Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
45	Write	DES	0x90	0x34	0x36	Disable auto acknowledge
						Initialize image sensor
46	Write	DES	0x90	0x34	0xB6	Enable auto ack -optional-
47	Read	SER	0x82	0x15		Verify valid PCLK -optional-
48	Read	SER	0x84	0x15		Verify valid PCLK -optional-
49	Read	SER	0x86	0x15		Verify valid PCLK -optional-
50	Read	SER	0x88	0x15		Verify valid PCLK -optional-

After the image sensor is initialized a valid PCLK can be read from register 0x15 of each serializer.

5. Enable GMSL & CSI-2

Enable all serial links using the broadcast address programmed into register 0x0B of all the serializers. I2C communication will not be available for 5ms while the GMSL links lock. Enable CSI-2 output after bit[6] of register 0x31 asserts frame synchronization is locked. Frame sync will require a minimum of two complete frames from the master link.

Table: GMSL/CSI-2 Enable Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
A	Write	SER	0x8A	0x06	0xAX	Set all devices Preemphasis settings (if needed)
B	Delay				5ms	I2C unavailable while GMSL locks
C	Write	DES	0x90	0x32, 0x33	0xXX	Set Deserializer Equalizer settings (if needed)
D	Write	DES	0x90	0x1B	0x0F	Enable EQs (if needed)
E	Delay				5ms	I2C unavailable while GMSL locks
F	Write	SER	0x8A	0x07	0xXX	Set EDC, for all devices (if needed)
G	Delay				2ms	Wait 2ms for I2C to clear (Step F causes loss of Lock)
H	Write	SER	0x90	0x0C	0xXX	Set EDC, for all devices (if needed)
I	Delay				5ms	I2C unavailable while GMSL locks
51	Write	SER	0x8A	0x04	0x83	Enable all serial links
52	Delay				5ms	I2C unavailable while GMSL locks
53	Read	DES	0x90	0x31		Poll frame synchronization bit
54	Write	DES	0x90	0x15	0x0B	Enable CSI-2 output

6. Verification

Along with programmed registers all status register are available for confirmation. Important status registers include pixel count, master link VSYNC period, and frame sync error counter.

Table: Verification Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
55	Read	DES	0x90	0x4D		GMSL link 0 pixel count
56	Read	DES	0x90	0x4E		
57	Read	DES	0x90	0x51		GMSL link 1 pixel count
58	Read	DES	0x90	0x52		
59	Read	DES	0x90	0x55		GMSL link 2 pixel count
60	Read	DES	0x90	0x56		
61	Read	DES	0x90	0x59		GMSL link 3 pixel count
62	Read	DES	0x90	0x5A		
63	Read	DES	0x90	0x5B		Calculated VSYNC period base on master link in terms of PCLK
64	Read	DES	0x90	0x5C		
65	Read	DES	0x90	0x5D		
66	Read	DES	0x90	0x5E		Frame sync error counter

Important Registers

The following Table Includes information on registers used in the programming applications, and other important registers.

Table: Important Serializer Registers

DEVICE		**MAX9271 SERIALIZER**	
REGISTER	**BIT**	**NAME**	**FUNCTION**
0x00	7:1	SERID	I2C Slave Address Set as a unique slave address. Serializer will respond to new address
0x04	7	SEREN	Enable serial link. Valid PCLK needed
	6	CLINKEN	Configuration Link Enable. Need for ACK's and I2C read back without GMSL locked
0x07	7	DBL	Double input mode 1 = RAW or YUV 0 = RAW
	4	ES	Data latched rising / falling edge of PCLK
	2	HVEN	HS/VS Encoding.
0x08	3	REV_LOGAIN	Reverse Channel Receiver Low Gain Enable
	0	REV_HIVTH	Reverse Channel Receiver High Threshold Enable
0x09	7:1	I2CSRCA	Source A I2C slave address Set as unique image sensor slave address
0x0A	7:1	I2CDSTA	Translated A I2C slave Address Set a local image sensor slave address
0x0B	7:1	I2CSRCB	Source B I2C slave address Set as unique serializer broadcast slave address
0x0C	7:1	I2CDSTB	Translated B I2C slave Address New serializer slave address. Same as register 0x00

Table: Important Deserializer Registers

DESERIALIZER		**MA9286 DESERIALIZER**	
REGISTER	**BIT**	**NAME**	**FUNCTION**
0x00	7:5	MST_LINK_SEL	Master link selection. All Frame sync timing based on master link. Auto = First GMSL link to lock
	4	EN_VS_GEN	0 = Disable internal VSYNC generation. Free running VSYNC used from camera 1 = Enable internal VSYNC generation. Frame sync base on registers 0x06 - 0x08
	3	LINK_EN_3	Enable GMSL link 3
	2	LINK_EN_2	Enable GMSL link 2
	1	LINK_EN_1	Enable GMSL link 1
	0	LINK_EN_0	Enable GMSL link 0
0x01	7:6	FSYNC_MODE	00 = Internally generate frame sync. FSYNC pin HIZ 01 = Internally generated frame sync. FSYNC pin outputs frame sync 10 = Slave MAX9286 receives frame sync from master MAX9286 on FSYNC 11 = MAX9286 receives frame sync from ECU on FSYNC
	1:0	FSYNCMETH	00 = Internal frame sync uses manual mode based on registers 0x06 - 0x08 01 = Semi - Auto: Used for image sensors which reset row pointers on FSIN 1X = Auto: Used for image sensors which reset row and column pointers on FSIN
0x06	7:0	FSYNC Period[7:0]	Manual mode of internally generated frame sync base on master link PCLK cycles
0x07	7:0	FSYNC Period[15:8]	

DESERIALIZER		**MA9286 DESERIALIZER**	
REGISTER	**BIT**	**NAME**	**FUNCTION**
0x08	7:0	FSYNC Period[23:16]	
0x0A	7	FWDCCEN3	Mask respective GMSL receive link for control channel communication
	6	FWDCCEN2	
	5	FWDCCEN1	
	4	FWDCCEN0	
	3	REVCCEN3	Mask respective GMSL transmit link for control channel communication
	2	REVCCEN2	
	1	REVCCEN1	
	0	REVCCEN0	
0x0C	7	HVEN	Use HS /VS encoding
	3	INVVS	Invert Vsync in CSI output
	2	INVHS	Invert Hsync in CSI output
0x12	7:6	CSILANCNT	00 = Enable CSI data lane D0 01 = Enable CSI data lane D0, D1 10 = Enable CSI data lane D0, D1, D2 11 = Enable CSI data lane D0, D1, D2, D3
	5	CSIDBL	CSI is single or double data rate
	4	DBL	0 = RAW (Single clock per pixel) 1 = YUV (Two clocks per pixel)

DESERIALIZER		**MA9286 DESERIALIZER**	
REGISTER	**BIT**	**NAME**	**FUNCTION**
	3:0	DATATYPE	Set RGB, YUV, or RAW and bit width. Refer to register table in data sheet for other options 0011 = YUV 422 8-bit 0100 = YUV 422 10-bit 0101 = RAW 8/16 0110 = RAW 10/20 1000 = RAW 14
0x15	3	CSIOUTEN	Enable CSI output.
0x1B	3	ENEQ3	Enable equalizer for Link 3
	2	ENEQ2	Enable equalizer for Link 2
	1	ENEQ1	Enable equalizer for Link 1
	0	ENEQ0	Enable equalizer for Link 0
0x31	7	FSYNCLOSS OFLOCK	Loss of frame sync has occurred
	6	FSYNC LOCKED	All enabled GMSL links have synchronized.
0x34	7	I2CLOCACK	MAX9286 generates acknowledge when forward channel is not available
0x3B	5:4	REV_TRF	Reverse channel transmitter transition time.

DESERIALIZER		MA9286 DESERIALIZER	
REGISTER	**BIT**	**NAME**	**FUNCTION**
	3:1	REV_AMP	Reverse channel amplitude 000 = 30mV 001 = 40mV 010 = 50mV 011 = 60mV 100 = 70mV 101 = 80mV 110 = 90mV 111 = 100mV
	0	REV_AMP_X	Add 100mV to REV_AMP
0x3F	6	EN_REV_CFG	Enable custom parameters from register 0x3B
	5:0	REV_FLEN	Reverse channel first pulse length with respects to internal oscillator Default is 54 clock with a min of 20. Pulse length = (20 + REV_FLEN)
0x4D	7:0	PKT_PPL_0[7:0]	GMSL link 0 pixel count
0x4E	7:0	PKT_PPL_0[15:8]	
0x51	7:0	PKT_PPL_1[7:0]	GMSL link 1 pixel count
0x52	7:0	PKT_PPL_1[15:0]	
0x55	7:0	PKT_PPL_2[7:0]	GMSL link 2 pixel count
0x56	7:0	PKT_PPL_2[15:8]	
0x59	7:0	PKT_PPL_3[7:0]	GMSL link 3 pixel count
0x5A	7:0	PKT_PPL_3[15:0]	
0x5B	7:0	CAL_FRM_LEN[7:0]	Calculated Vsync period base on master link in terms of PCLK
0x5C	7:0	CAL_FRM_LEN[15:8]	

DESERIALIZER		**MA9286 DESERIALIZER**	
REGISTER	**BIT**	**NAME**	**FUNCTION**
0x5D	7:0	CAL_FRM_LEN[23:0]	
0x5E	7:0	FRM_SYNC_ERR_CNT	Frame sync error counter
0x69	5	AUTO_COMBACK_EN	Enable auto come back feature MAX9286 will create valid CSI timing for enabled GMSL link which are not valid.
	4	AUTO_MASK	Enable auto mask MAX9286 will automatically mask invalid GMSL link data stream

MAX9272 Programming Guide

Abstract: This document provides general setup procedures for the MAX9272 Gigabit Multimedia Serial Link (GMSL) Deserializer.

Introduction

The MAX9272 GMSL deserializer receives data over 50Ω coax or 100Ω shielded twisted pair (STP) cables. Programming can be divided into 6 parts, each of will be dealt with separately.

1. **Reverse Channel Setup**
2. **MAX9272 Initial Setup**
3. **GMSL Link Setup**
4. **Image Sensor Initialization**
5. **Enable GMSL**
6. **Verification**

Setup Sequence Example for MAX9272, MAX9271

1. *Reverse Channel Setup*

It is important to establish a robust I2C connection between the deserializer and serializer. With the addition of power over coax, and an inherently noisy environment; default reverse channel settings will need to be adjusted. After power up it is important to adjust the deserializer's amplitude and the serializer's input levels before any other I2C transactions to avoid unwanted effects on the serializers I2C registers.

Table: Reverse Channel Setup Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
1	Write	DES	0x90	0x15	0x17	First pulse length rise time changed from 300ns to 200ns
2	Delay				2ms	Wait 2ms after any change to reverse channel settings *Note 2
3	Write	SER	0x80	0x04	0x43	Optional - Enable configuration link *Note 1
4	Delay				5ms	Wait 5ms for configuration link to establish
5	Write	SER	0x80	0x08	0x01	Enable high threshold for reverse channel input buffer. This increases immunity to power supply noise when the coaxial link is used for power as well as signal.
6	Delay				2ms	Wait 2ms after any change to reverse channel settings *Note 2
7	Write	DES	0x90	0x15	0x1F	Increase reverse amplitude from 100mV to 160mV. This compensates for the higher threshold of step 5.
8	Delay				2ms	Wait 2ms after any change to reverse channel settings *Note 2

***Note 1:** Lines 7 & 8 are only needed for Acknowledge or I2C read back from the serializer when there is no PCLK to establish the forward link.

***Note 2:** 2ms of delay is needed after any analog change to the reverse channel for bus timeout and for the I2C state machine to settle from any glitches.

***Note 3:** The control channel cannot be used while establishing a link, 5ms of delay is required to establish the configuration link.

2. MAX9272 Initial Setup

After reverse channel settings the output can be disabled until Lock is achieved. Register 0x07 selects the GMSL Double Mode, BWS and output clock edge. MAX9272 DBL=0 for RAWx1 or DBL=1 or RAWx2 / YUV 422.

Table: MAX9272 Initial Setup Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
9	Write	DES	0x90	0x04	0x47	Disable output
10	Write	DES	0x90	0x07	0x84	Enable DBL mode Enable HS/VS encoding All other bits at default state

3. GMSL Link Setup

If multiple links are used in the application, and if all links share an I2C bus, then each serializer and deserializer needs to be setup individually and their respective I2C slave address changed to a unique value. All the MAX9271's and MAX9272s will power up with the same slave address. To combat this Power up one deserializer at a time via register the individual PWDN pins and change the MAX9272 slave address in register 0x01. If the image sensors have the same slave address the I2C translation registers 0x09 & 0x0A can be utilized to create a unique I2C slave address. The same approach can be applied to create a MAX9271 broadcast slave address. Simply write the broadcast address to register 0x0B and the respective MAX9271 address to register 0x0C. (see the table below)

Table: Example MAX9271 Address Translation Register Settings

MAX9271	REG 0X00	REG 0x09	REG 0x0A	REG 0x0B	REG 0x0C
Link 0	0x82	0x62	0x60	0x8A	0x82
Link 1	0x84	0x64	0x60	0x8A	0x84
Link 2	0x86	0x66	0x60	0x8A	0x86

Link 3	0x88	0x68	0x60	0x8A	0x88

Note: Keep the default serializer and deserializer address 0x80/0x90 reserved to allow easy detection and initialization in case of a Power-on-reset in one of the camera modules or deserializers

Table: I2C Address Setup for Multiple Deserializers

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
A	PWDN = high	DES				Power on first MAX9272 deserializer
B	Delay	DES			6ms	Wait 6ms for device to power up
C	Write	DES	0x90	0x01	0x92	Change deserializer slave address to 0x92
D	Repeat					Repeat steps A through C for all other deserializers (assign a unique deserializer address for each

Note: Do steps A through D first before any other setup steps

Table: GMSL Link Setup Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
11	Write	DES	0x92	0x04	0x44	Disable Control channel at serializer address 0x92
12	Delay				2ms	Wait 2ms after any change to reverse channel settings
13	Repeat					Repeat Steps 11 and 12 for all other deserializers
14	Write	DES	0x92	0x04	0x47	Enable Link 1 Reverse Channel
15	Write	SER	0x80	0x00	0x82	Change serializer slave address to 0x82
16	Write	SER	0x82	0x07	0x94	Enable DBL Set Edge Select 1=Rise / 0=Fall Enable HS/VS encoding

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
17	Write	SER	0x82	0x09	0x62	Unique Link 1 image sensor slave address 0x62
18	Write	SER	0x82	0x0A	0x60	Link 1 image sensor slave address
19	Write	SER	0x82	0x0B	0x8A	Serializer broadcast address 0x7A
20	Write	SER	0x82	0x0C	0x81	Link 1 serializer address
21	Repeat					Repeat steps 14 to 21 for all other links

4. Image Sensor Initialization

Two feedback approaches can be taken when initializing the image sensor. Read back after each write or utilize I2C acknowledge. Both will require the configuration link to be enabled in step 7. For I2C acknowledge method disable auto ACK in register 0x0D of MAX9272.

Table: Image Sensor Initialization Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
22	Write	DES	0x92	0x0D	0x36	Disable auto acknowledge
23	Repeat					Repeat for all deserializers
23						Initialize image sensor
24	Write	DES	0x92	0x0D	0xB6	Enable auto ack -optional-
25	Repeat					Repeat for all deserializers
26	Read	SER	0x82	0x15		Verify valid PCLK -optional-
27	Repeat					Repeat for all serializers

After the image sensor is initialized a valid PCLK can be read from register 0x15 of each serializer.

5. Enable GMSL

Enable all serial links using the broadcast address programmed into register 0x0B of all the serializers. I2C communication will not be available for 5ms while the GMSL links lock.

Table: GMSL Enable Procedure

STEP	OPERATION	DEVICE	SLAVE ID	REGISTER	VALUE	DESCRIPTION
A	Write	SER	0x8A	0x06	0xAX	Set all devices Preemphasis settings (if needed)
B	Delay				5ms	I2C unavailable while GMSL locks
C	Write	DES	0x9x	0x05	0x3X	Set Deserializer Equalizer settings (if needed)
D	Delay				5ms	I2C unavailable while GMSL locks
E	Repeat					Repeat C-D for all deserializers
F	Write	SER	0x8A	0x07	0xXX	Set EDC, for all devices (if needed)
G	Delay				2ms	Wait 2ms for I2C to clear (Step F causes loss of Lock)
H	Write	SER	0x9X	0x07	0xXX	Set EDC, for all devices (if needed)
I	Delay				5ms	I2C unavailable while GMSL locks
J	Repeat					Repeat H-I for all deserializers
28	Write	SER	0x8A	0x04	0x83	Enable all serial links
29	Delay				5ms	I2C unavailable while GMSL locks
30	Write	DES	0x92	0x04	0x07	Enable outputs
31	Repeat					Repeat for all deserializers

Important Registers

The following Table Includes information on registers used in the programming applications, and other important registers.

Table: Important Serializer Registers

DEVICE		MAX9271 SERIALIZER	
REGISTER	**BIT**	**NAME**	**FUNCTION**
0x00	7:1	SERID	I2C Slave Address Set as a unique slave address. Serializer will respond to new address
0x04	7	SEREN	Enable serial link. Valid PCLK needed
	6	CLINKEN	Configuration Link Enable. Need for ACK's and I2C read back without GMSL locked
0x07	7	DBL	Double input mode 1 = RAW or YUV 0 = RAW
	4	ES	Data latched rising / falling edge of PCLK
	2	HVEN	HS/VS Encoding.
0x08	3	REV_LOGAIN	Reverse Channel Receiver Low Gain Enable
	0	REV_HIVTH	Reverse Channel Receiver High Threshold Enable
0x09	7:1	I2CSRCA	Source A I2C slave address Set as unique image sensor slave address
0x0A	7:1	I2CDSTA	Translated A I2C slave Address Set a local image sensor slave address
0x0B	7:1	I2CSRCB	Source B I2C slave address Set as unique serializer broadcast slave address

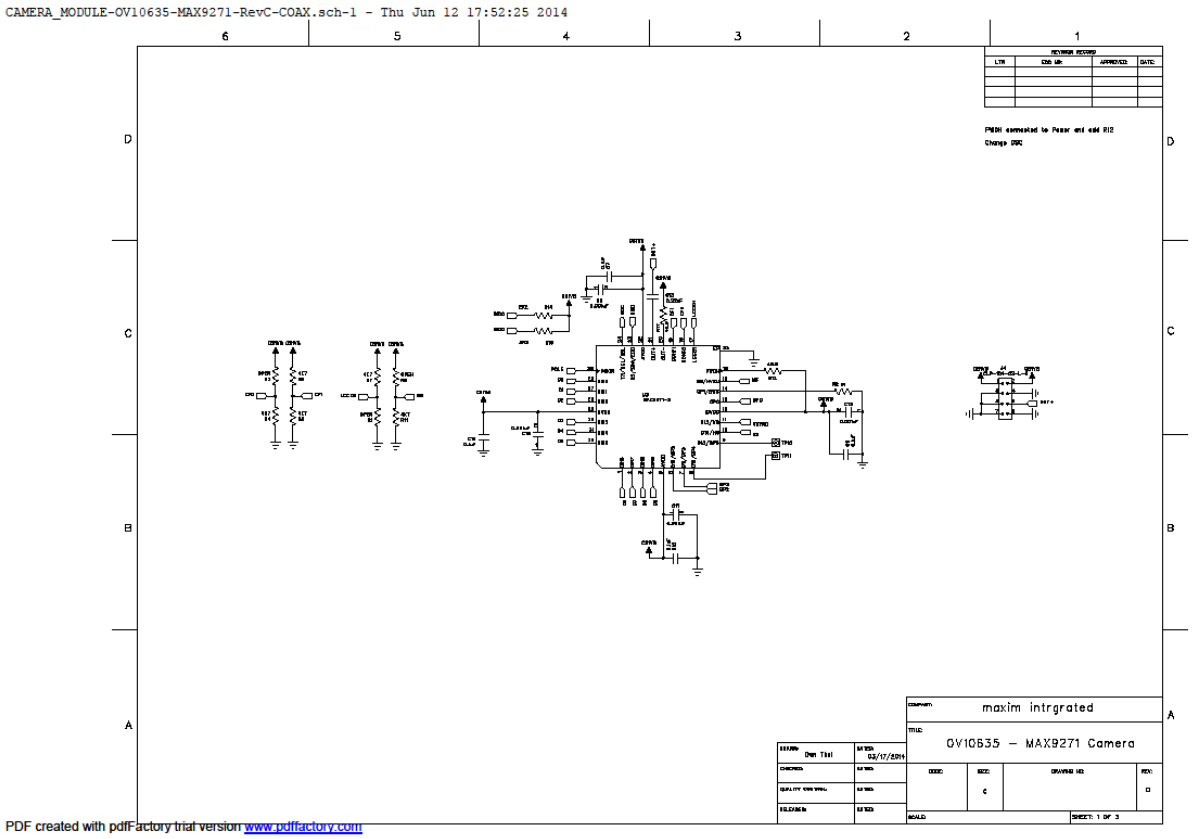
0x0C	7:1	I2CDSTB	Translated B I2C slave Address New serializer slave address. Same as register 0x00

Table: Important Deserializer Registers

DESERIALIZER		**MA9286 DESERIALIZER**	
REGISTER	**BIT**	**NAME**	**FUNCTION**
0x01	7:1	DESID	I2C Slave Address Set as a unique slave address. Serializer will respond to new address
0x04	7	LOCKED	LOCK output pin level
	1	REVCCEN	Enable reverse control channel from deserializer
	0	FWDCCEN	Enable forward control channel to deserializer
	4	SLEEP	Activate sleep mode
	3	REVCCEN	Enable reverse control channel from deserializer
	0	FWDCCEN	Enable forward control channel to deserializer
0x07	7	DBL	Double output mode (Default value is controlled by DBL pin when LCCEN=0) 0 = single input **(d)** 1 = double input
	6	BWS	Bus width select (Default value is controlled by BWS pin when LCCEN=0) 0 = 22-bit bus **(d)** 1 = 30-bit bus
	4	ES	Edge select (Default value is controlled by ES pin when LCCEN=0) 0 = rising edge **(d)** 1 = falling edge
	2	HVEN	HS/VS encoding enable (Default value is controlled by HVEN pin when LCCEN=0) 0 = disabled **(d)** 1 = enabled

DESERIALIZER		**MA9286 DESERIALIZER**	
REGISTER	**BIT**	**NAME**	**FUNCTION**
0x08	7	INV_VS	Invert VS at the output (inverts DOUT0 when HVEN=0)
	3	INV_HS	Invert HS at the output (inverts DOUT1 when HVEN=0)
0x13	7	I2CLOCACK	MAX9272 generates acknowledge when forward channel is not available
0x15	5:4	REV_TRF	Reverse channel transmitter transition time.
	3:0	REV_AMP	Reverse channel amplitude 0000 = 30 mV 1000 = 90 mV 0001 = 40 mV 1001 = 100 mV 0010 = 50 mV 1010 = 110 mV 0011 = 60 mV 1011 = 120 mV 0100 = 70 mV 1100 = 130 mV 0101 = 80 mV 1101 = 140 mV 0110 = 90 mV 1110 = 150 mV 0111 = 100 mV 1111 = 160 mV

Appendix: Reference Design



Right-click diagram to open