

R-CarM2N System Evaluation Board GOSE

Hardware Manual

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Contents

| | |
|--|----|
| 1. Overview | 1 |
| 1.1. Features | 1 |
| 1.1.1. The R-CarM2N includes: | 1 |
| 1.1.2. The GOSE board includes: | 2 |
| 1.2. Usage Notes | 4 |
| 1.2.1. GOSE Board Specifications | 4 |
| 1.3. Board Configuration | 5 |
| 1.3.1. Block Diagram of GOSE Board | 5 |
| 1.3.2. Address Map of GOSE Board | 6 |
| 2. GOSE Interface Module Specifications | 7 |
| 2.1. Mode Setting | 7 |
| 2.1.1. Specifications | 7 |
| 2.1.2. Initial Values of Mode Setting Pins on GOSE Board | 9 |
| 2.1.3. Multiplexing and Method of Setting for Mode Setting Pins | 10 |
| 2.1.4. Block Diagram of Peripheral Circuit for Mode Pins | 11 |
| 2.2. DDR3L-SDRAM Interface | 12 |
| 2.2.1. Specifications | 12 |
| 2.2.2. Signal Correlation | 12 |
| 2.2.3. Block Diagram | 13 |
| 2.3. Flash Memory Sub-Board Interface | 14 |
| 2.3.1. Specifications | 14 |
| 2.3.2. Block Diagram | 15 |
| 2.4. SPI-Flash Interface (QSPI) | 16 |
| 2.4.1. Specifications | 16 |
| 2.4.2. Block Diagram | 16 |
| 2.5. Video Input Interface | 17 |
| 2.5.1. Specifications | 17 |
| 2.5.2. Block Diagram | 17 |
| 2.6. Video Input Interface 0 | 18 |
| 2.6.1. Specifications | 18 |
| 2.6.2. Block Diagram | 18 |
| 2.7. Video Input Interface 1 | 19 |
| 2.7.1. Specifications | 19 |
| 2.7.2. Block Diagram | 19 |
| 2.8. Video Output Interface | 20 |
| 2.8.1. Specifications | 20 |
| 2.8.2. Block Diagram | 21 |
| 2.9. MediaLB 6-pin/3-pin Interface | 22 |
| 2.9.1. Specifications | 22 |
| 2.9.2. Block Diagram | 22 |
| 2.10. Debugger Interface | 23 |
| 2.10.1. Specifications | 23 |
| 2.10.2. Block Diagram | 23 |
| 2.11. Debug Ether Interface (EtherMAC) | 24 |
| 2.11.1. Specifications | 24 |
| 2.11.2. Block Diagram | 24 |
| 2.12. Audio Codec Interface (SSI0, SSI1, SSI2, and SSI9, or SSI3 and SSI4) | 25 |
| 2.12.1. Specifications | 25 |
| 2.12.2. Block Diagram | 25 |
| 2.13. Serial-ATA Interface | 27 |

| | | |
|---------|--|----|
| 2.13.1. | Specifications..... | 27 |
| 2.13.2. | Block Diagram..... | 27 |
| 2.13.3. | Serial-ATA Clock Source Unit | 27 |
| 2.14. | SD Card Host Interface 0 (SDHI0) | 28 |
| 2.14.1. | Specifications..... | 28 |
| 2.14.2. | Block Diagram..... | 28 |
| 2.15. | SD Card Host Interface 1 (SDHI1) | 29 |
| 2.15.1. | Specifications..... | 29 |
| 2.15.2. | Block Diagram..... | 29 |
| 2.16. | SD Card Host Interface 2 (SDHI2) | 30 |
| 2.16.1. | Specifications..... | 30 |
| 2.16.2. | Block Diagram..... | 30 |
| 2.17. | USB2.0 Interface | 31 |
| 2.17.1. | Specifications..... | 31 |
| 2.17.2. | Block Diagram..... | 31 |
| 2.18. | Debug Serial Interfaces (SCIF0 and SCIF1)..... | 32 |
| 2.18.1. | Specifications..... | 32 |
| 2.18.2. | Block Diagram..... | 32 |
| 2.19. | External RTC (I ² C Bus Interface) | 33 |
| 2.19.1. | Specifications..... | 33 |
| 2.19.2. | Block Diagram..... | 33 |
| 2.20. | Reset | 34 |
| 2.20.1. | Specifications..... | 34 |
| 2.20.2. | Block Diagram..... | 34 |
| 2.21. | I ² C Interface | 35 |
| 2.21.1. | Specifications..... | 35 |
| 2.21.2. | List of Slave Addresses | 36 |
| 2.21.3. | Block Diagram..... | 37 |
| 2.22. | GPIO Interface (Software Switch, Tactile Switches, and General-Purpose LEDs) | 38 |
| 2.22.1. | Specifications..... | 38 |
| 2.22.2. | Block Diagram..... | 38 |
| 2.23. | External Wait..... | 39 |
| 2.23.1. | Specifications..... | 39 |
| 2.23.2. | Block Diagram..... | 39 |
| 2.24. | External Interrupts | 40 |
| 2.24.1. | Specifications..... | 40 |
| 2.24.2. | Block Diagram..... | 40 |
| 2.25. | PWM..... | 41 |
| 2.26. | TCLK for External Clock Input..... | 41 |
| 2.27. | Clock..... | 42 |
| 2.27.1. | Clocks Supplied to the R-CarM2N | 42 |
| 2.27.2. | Clocks Supplied to Devices Other than R-CarM2N | 42 |
| 2.28. | Power Supply | 43 |
| 2.28.1. | Specifications..... | 43 |
| 2.28.2. | Block Diagram..... | 44 |
| 2.28.3. | Power-On Sequence..... | 45 |
| 2.29. | EXIO Connectors (CN30, CN31, CN32, CN33, and CN34) | 46 |
| 2.29.1. | Specifications..... | 46 |
| 3. | Outline Diagrams of GOSE Board | 49 |
| 3.1. | External Dimensions and Hole Locations of GOSE Board..... | 49 |
| 3.2. | Connector Locations on GOSE Board (Component Surface) | 50 |

| | | |
|------|---|----|
| 3.3. | Connector Locations on GOSE Board (Solder Surface)..... | 51 |
|------|---|----|

Tables

| | |
|--|----|
| Table 1.1.1 List of GOSE Board Functions (1)..... | 2 |
| Table 1.1.2 List of GOSE Board Functions (2)..... | 3 |
| Table 2.1.1 Initial Values of R-CarM2N Mode Setting Pins on GOSE Board | 9 |
| Table 2.1.2 Pin Multiplexing of Mode Setting Pins of R-CarM2N | 10 |
| Table 2.2.1 DDR3L-SDRAM Specifications | 12 |
| Table 2.2.2 DDR3L-SDRAM Signal Correlation | 12 |
| Table 2.3.1 Flash Memory Sub-Board Specifications | 14 |
| Table 2.4.1 SPI-FLASH Interface Specifications..... | 16 |
| Table 2.5.1 Video Input Specifications..... | 17 |
| Table 2.8.1 Video Output Interface Specifications | 20 |
| Table 2.9.1 MediaLB Connector Pin List | 22 |
| Table 2.9.2 MediaLB Connector Specification..... | 22 |
| Table 2.10.1 DBG Specifications | 23 |
| Table 2.11.1 Debug Ether Interface Specifications | 24 |
| Table 2.12.1 SSI Codec Specifications..... | 25 |
| Table 2.12.2 SSI Connections on the GOSE Board..... | 26 |
| Table 2.13.1 Serial-ATA Interface Specifications | 27 |
| Table 2.14.1 SD Card Host Interface (SDHI0) Specifications | 28 |
| Table 2.15.1 SD Card Host Interface (SDHI1) Specifications | 29 |
| Table 2.16.1 SD Card Host Interface (SDHI2) Specifications | 30 |
| Table 2.17.1 USB2.0 Specifications..... | 31 |
| Table 2.18.1 Debug Serial Interface Specifications..... | 32 |
| Table 2.19.1 External RTC (I ² C) Specifications | 33 |
| Table 2.20.1 RESET Specifications | 34 |
| Table 2.21.1 I ² C Interface Specifications..... | 35 |
| Table 2.21.2 List of I ² C Slave Addresses | 36 |
| Table 2.22.1 List of Software Switch (General-Purpose Switch) | 38 |
| Table 2.22.2 List of Tactile Switches (General-Purpose Switches) | 38 |
| Table 2.22.3 List of General-Purpose LEDs..... | 38 |
| Table 2.23.1 External Wait Control Interface Specifications | 39 |
| Table 2.24.1 External Interrupt Specifications..... | 40 |
| Table 2.25.1 Pin Functions Given Priority over PWM Functions | 41 |
| Table 2.26.1 Pin Functions Given Priority over TCLK Functions..... | 41 |
| Table 2.27.1 List of Clocks and Crystals for R-CarM2N | 42 |
| Table 2.27.2 List of Clocks and Crystals Other than for R-CarM2N | 42 |
| Table 2.28.1 List of GOSE Board Switching Controllers and Regulators | 43 |
| Table 2.29.1 EXIO Connector Specifications..... | 46 |
| Table 2.29.2 List of EXIO Connector A (CN31) Pins..... | 46 |
| Table 2.29.3 List of EXIO Connector B (CN32) Pins | 47 |
| Table 2.29.4 List of EXIO Connector C (CN33) Pins | 47 |
| Table 2.29.5 List of EXIO Connector D (CN34) Pins | 48 |
| Table 2.29.6 List of EXIO Connector E (CN30) Pins..... | 48 |

Figures

| | |
|--|----|
| Figure 1.3.1 Block Diagram of GOSE Board..... | 5 |
| Figure 1.3.2 Address Map of GOSE Board..... | 6 |
| Figure 2.1.1 Peripheral Circuit for Mode Pins on GOSE Board | 11 |
| Figure 2.2.1 Block Diagram of DDR3L-SDRAM Interface | 13 |
| Figure 2.3.1 Block Diagram of Flash Memory Sub-Board Interface | 15 |
| Figure 2.4.1 Block Diagram of SPI-Flash Interface | 16 |
| Figure 2.5.1 Block Diagram of Video Input Interface | 17 |
| Figure 2.6.1 Block Diagram of Video Input Interface 0..... | 18 |
| Figure 2.7.1 Block Diagram of Video Input Interface 1..... | 19 |
| Figure 2.8.1 Block Diagram of Video Output Interface | 21 |
| Figure 2.9.1 Block Diagram of MediaLB Interface..... | 22 |
| Figure 2.10.1 Block Diagram of JTAG (DBG) Interface | 23 |
| Figure 2.10.2 Block Diagram of SDHI1 Slot Debugger (DBG2) Interface | 23 |
| Figure 2.11.1 Block Diagram of Debug Ether Interface | 24 |
| Figure 2.12.1 Block Diagram of Audio Codec Interface..... | 25 |
| Figure 2.13.1 Block Diagram of Serial-ATA Interface | 27 |
| Figure 2.13.2 Block Diagram of Serial-ATA Clock Source..... | 27 |
| Figure 2.14.1 Block Diagram of SD Card Host Interface (SDHI0) | 28 |
| Figure 2.15.1 Block Diagram of SD Card Host Interface (SDHI1) | 29 |
| Figure 2.16.1 Block Diagram of SD Card Host Interface (SDHI2) | 30 |
| Figure 2.17.1 Block Diagram of USB2.0 Interface | 31 |
| Figure 2.18.1 Block Diagram of Debug Serial Interface..... | 32 |
| Figure 2.19.1 Block Diagram of External RTC Connection | 33 |
| Figure 2.20.1 Block Diagram of Reset Circuit | 34 |
| Figure 2.21.1 Block Diagram of I ² C Interfaces | 37 |
| Figure 2.22.1 Block Diagram of GPIO Interface (Software Switch, Tactile Switches, and General-Purpose LEDs)..... | 38 |
| Figure 2.23.1 Block Diagram of External Wait Interface | 39 |
| Figure 2.24.1 Block Diagram of External Interrupts | 40 |
| Figure 2.28.1 Block Diagram of Power Supply..... | 44 |
| Figure 2.28.2 Power-On Sequence..... | 45 |
| Figure 3.1.1 External Dimensions and Hole Locations of the GOSE Board..... | 49 |
| Figure 3.2.1 Connector Locations of the GOSE Board (Component Surface)..... | 50 |
| Figure 3.3.1 Connector Locations of the GOSE Board (Solder Surface) | 51 |

1. Overview

The R-CarM2N is a new generation SOC featuring the basic functionality required for the next generation of car navigation systems. Its newly employed bus configuration maximizes the system performance, space saving, and cost efficiency.

The GOSE is an R-CarM2N-specific evaluation board that can be used to evaluate systems using the R-CarM2N and to develop operating systems, device drivers, and applications. Using the GOSE board allows the developers to efficiently conduct required tasks such as evaluation of the R-CarM2N system performance and thus greatly to reduce the turn-around time in their product development.

1.1. Features

1.1.1. The R-CarM2N includes:

- Two 1.5-GHz ARM Cortex™-A15 MPCore™ cores
- Multimedia Engine SH-4A: 780 MHz
- Memory controller for DDR3-SDRAM (DDR3-1600) with 32 bits
- 3DGE, R-GP 2D, DU (LVDS 1ch and digital RGB 1ch), DCU, TCON, VIN (2ch), IMR-LSX2
- VSP1, VCP3, FDP1, 2D-DMAC, JPU, SSP1 (option)
- ADSP, SCU, SSIU (10ch), MediaLB+, MLM, DTCP, ADG
- Crypto Engine
- USB2.0 Host, USB2.0 Host/Function
- USB3.0 Host (SuperSpeed), Serial-ATA, PCI-Express
- SDHI (3ch), MMCIF
- CAN (2ch), IE-BUS, EthernetMAC, EthernetAVB
- WDT, TPU, CMT1, TMU, CPG, INTC, DMAC, LBSC
- I²C (5ch), SCIF (6ch), SCIFA (6ch), SCIFB (3ch), MSIOF (3ch), QSPI, HSCIF (3ch), PWM (7ch)
- Gyro ADC I/F, Speed-pulse I/F, TSIF, REMOCON, DARC, GPS
- SIM card (option), GPIO, etc.
- Power supply voltage (typ.): 3.3 V, 1.8 V, 1.5 V/1.35 V, 1.0 V
- Operating temperature: +25 degrees C at ambient temperature

1.1.2. The GOSE board includes:

Table 1.1.1 List of GOSE Board Functions (1)

| The GOSE board Function List. Page 1 of 2 | | | |
|---|-------------------|---|--|
| Board Function | Module | Description | Note |
| RAM | DDR3 | Single Channel DDR3L-1600, 1GByte x1 channels, 32bit data width x1 channels 4Gbit(16bit data width) x2 devices. SDRAM Backup feature: Supported. | |
| | LBSC | No device. | |
| ROM | LBSC | NOR Flash Connector: NOR Flash board: R0P0400C0001FS Databus width 16bit 64MB x2banks or 128MB x1bank | Pin Multi: QSPI For Interrupt: IRQ1 |
| | QSPI | SPI Flash: Spansion S25FL512SAGMFIG11 (512Mbit=64MB) x1 device. Spansion S25FL032P0XMF1011 (32Mbit=4MB) x1 device. | Pin Multi: LBSC_A[25:20] |
| Debug I/F | DBG | Connector: HTST-110-01-S-DV (20pin) | |
| | DBG2 | through SD card slot for SDHI1 | |
| | GPIO | LED x3 devices 'GPLED' for General Purpose. | GPIOs: GP2_19 ~ GP2_21 |
| | | Mechanical switch x4 elements ' SOFTSW ' for General Purpose. | GPIOs: GP5_0 ~ GP5_3 |
| | | Mechanical switch x7 elements ' TactSW ' for General Purpose. | GPIOs: GP7_0 ~ GP7_6 |
| | SCIF0 | Debug Serial x1 (TX, RX) USB to UART Bridge SILICON LABS CP2102-GM x1 (Bridge spec: max 1Mbps) Connector: USB Type microAB | |
| LAN | SCIF1 | Debug Serial x1 (TX, RX) USB to UART Bridge SILICON LABS CP2102-GM x1 (Bridge spec: max 1Mbps) Connector: USB Type microAB | |
| | EtherMAC | Debug Ether(100Mbps) RMII PHY: MICREL KSZ8041RNLJ Connector: TDK TLA-6T776F EXIO Connector D (CN34 : QSE-040-01-F-D-A) | For Interrupt: IRQ0 For Reset: GP5_22 Pin Multi: EtherAVB |
| SATA I/F | SATA0 | 3Gbps, Gen2 Connector: 67491-0020 | Pin Multi: USB3.0 / PCIE |
| USB2.0 I/F | USB2.0 ch0 | USB2.0 Host or Function Connector: Type microAB. | |
| | USB2.0 ch1 | USB2.0 Host Connector: Type A. | |
| MLB+ I/F | MLB+ (MOST) | 6wire-MOST Interface(150Mbps) Connector: QSH-020-01-L-D-DP-A | |
| RTC I/F | I ² C1 | Real Time Clock: SEIKO EPSON RA-8581SA (Not mounted, only pad) | There is no device on the board. For Interrupt: IRQ1 |
| SDHI | SDHI0 | Connector: SD Card slot. Interface voltage: Either 3.3V or 1.8V. | For voltage control: GP2_12, GP7_17 |
| | SDHI1 | Connector: SD Card slot. DBG2 can be connected instead of SD card. Interface voltage: Either 3.3V or 1.8V. | For voltage control: GP2_13, GP7_18 |
| | SDHI2 | Connector: microSD Card slot. Either 3.3V or 1.8V. | For voltage control: GP2_26, GP7_19 MMC |
| MSIOF | MSIOF0 | Renesas Electronics R2A11302FT Connectotr: EXIO Connector B (CN32 : QSE-040-01-F-D-A) | |
| Video Output | DU0_LVDS | LVDS output. 5 pair (CLK, CH0 ~ CH3) Connector: Signal: Hirose DF14A-20P-1.25H(55), Backlight: JST SM14B-SRSS-TB(LF)(SN) | |
| | DU1 | Either [A] or [B] [A] HDMI output HDMI Transmitter.ADV7511WBSWZ Connector: Type A Receptacle: Tyco 1747981-1 [B] Connector: EXIO Connector E (CN30 : QSE-020-01-F-D-A) | For Interrupt: GP3_29 |
| Video Input | VIN0 | Either [A] or [B] [A] YCbCr 16bit. RGB888 HDMI Reciever: Analog Devices ADV7612WBSWZ. Connector:Type A Receptacle [B] Connector: EXIO Connector D (CN34 : QSE-040-01-F-D-A) | For Interrupt: GP4_2 |
| | VIN1 | Either [A] or [B] [A] YCbCr 8bit. BT656 Video Decoder: Analog Devices ADV7180WBCP32Z, Connector: RCA [B] Connector: EXIO Connector D (CN34 : QSE-040-01-F-D-A) | Pin Multi: EtherAVB |

Table 1.1.2 List of GOSE Board Functions (2)

| The GOSE board Function List. Page 2 of 2 | | | |
|---|------------------------|--|--|
| Board Function | Module | Description | Note |
| Audio | SSI0, SSI1, SSI2, SSI9 | <p>Either [A1] or [B] or [C] or [D]</p> <p>[A1] Audio Output(SSI0), Input(SSI1) Codec: AKM AK4643EN x1 Connector: mini jack x1 for stereo line output Connector: mini jack x1 for stereo line/MIC input</p> <p>[B] Audio Multi-Channel Output.(SSI0, SSI1, SSI2, SSI9) HDMI Transmitter ADV7511WBSWZ Connector: HDMI standard type A</p> <p>[C] Audio Multi-Channel Input(SSI0, SSI1, SSI2, SSI9) or TDM Input(SSI0) HDMI Receiver ADV7612WBSWZ Connector: HDMI standard type A</p> <p>[D] Connector: samtec 80pin. EXIO Connector B (CN32 : QSE-040-01-F-D-A)</p> | Note: SSI channels connected to AK4643 can be selected by 0 Ω register.(Initial setting) |
| | SSI3, SSI4 | <p>[A2] Audio Output(SSI3), Input(SSI4) Codec: AKM AK4643EN x1 Connector: mini jack x1 for stereo line output Connector: mini jack x1 for stereo line/MIC input EXIO Connector B (CN32 : QSE-040-01-F-D-A)</p> | Note: SSI channels connected to AK4643 can be selected by 0 Ω register. |
| I ² C I/F | I ² C1 | <p>Interface voltage: 3.3V This interface is connected to the following devices. PMIC DA9063, RTC RA-8581SA and EXIO Connector B (CN32 : QSE-040-01-F-D-A)</p> | |
| | I ² C2 | <p>Interface voltage: 3.3V This interface is connected to the following devices. HDMI Transmitter ADV7511, HDMI Receiver ADV7612, Video decoder ADV7180, Audio codes AK4643, I2C EEPROM, EXIO Connector A (CN31: QSE-040-01-F-D-A) and EXIO Connector D (CN34: QSE-040-01-F-D-A)</p> | |
| | I ² C4 | <p>Interface voltage: 3.3V This interface is connected to the following devices. Pin header (CN28 : DSP03-004-432G) and EXIO Connector E (CN30 : QSE-020-01-F-D-A)</p> | Note: The DSP03-004-432G is not mounted. |
| | I ² C5 | <p>Interface voltage: 1.8V Pin header (CN29 : DSP03-004-432G)</p> | Note: The DSP03-004-432G is not mounted. |
| | I ² C6 | <p>Interface voltage: 1.8V This interface is connected to the following devices. PMIC DA9063, DA9210 and EXIO Connector C (CN33 : QSE-020-01-F-D-A)</p> | |
| EXIO Connector | various modules | <p>EXIO Connector A CN31 samtec 80pin.QSE-040-01-F-D-A</p> <p>EXIO Connector B CN32 samtec 80pin.QSE-040-01-F-D-A</p> <p>EXIO Connector C CN33 samtec 40pin.QSE-020-01-F-D-A</p> <p>EXIO Connector D CN34 samtec 80pin.QSE-040-01-F-D-A</p> <p>EXIO Connector E CN30 samtec 40pin.QSE-020-01-F-D-A</p> | |
| Power IC | — | <p>Renesas Electronics R2A11302FT, HAT2210R</p> <p>Dialog Semiconductor DA9210, DA9063</p> <p>Linear Technology LTC3634EFE#PBF</p> | |
| Power Supply | — | DC12.0V input | |
| Board size | — | 210mm x 160mm | |

1.2. Usage Notes

1.2.1. GOSE Board Specifications

- Take particular care to ensure the correct configurations of the jumpers and switches mounted on the GOSE board. Incorrect configurations may damage on-board devices.
- For the GOSE board, be sure to use the power supply that comes with it. Applying a voltage greater than 12 V may damage devices on the GOSE board.
- There are sequences for turning on and off the power supply to the R-CarM2N. For the GOSE board, be sure to obey the notes below.
 - (1) When power is turned on
 - Be sure to confirm that the ACC switch (SW25) is off before plugging the AC adapter into the power source.
 - It is prohibited to plug the AC adapter into a power source while the ACC switch (SW25) is on.
 - (2) When power is shut off
 - Be sure to turn off the ACC switch (SW25) before unplugging the AC adapter from the power source.
 - It is prohibited to unplug the AC adapter from the power source while the ACC switch (SW25) is on.
- The typical default value for overcurrent detection by the power IC (R2A11302FT) is defined as 7 A in the specifications. The maximum current drawn by the VSYS and D5.0V pins on the GOSE board is thus 7 A each. Therefore, operation should be such that the current drawn by either pin does not exceed 7 A. Also ensure that the current drawn does not exceed 7 A if an IO expansion board or external storage device is connected to the GOSE board.

1.3. Board Configuration

The GOSE board is composed of a single board whose size is 210 mm × 160 mm.

Figure 1.3.1 shows a block diagram of the GOSE board.

Figure 1.3.2 is a memory map of the GOSE board.

1.3.1. Block Diagram of GOSE Board

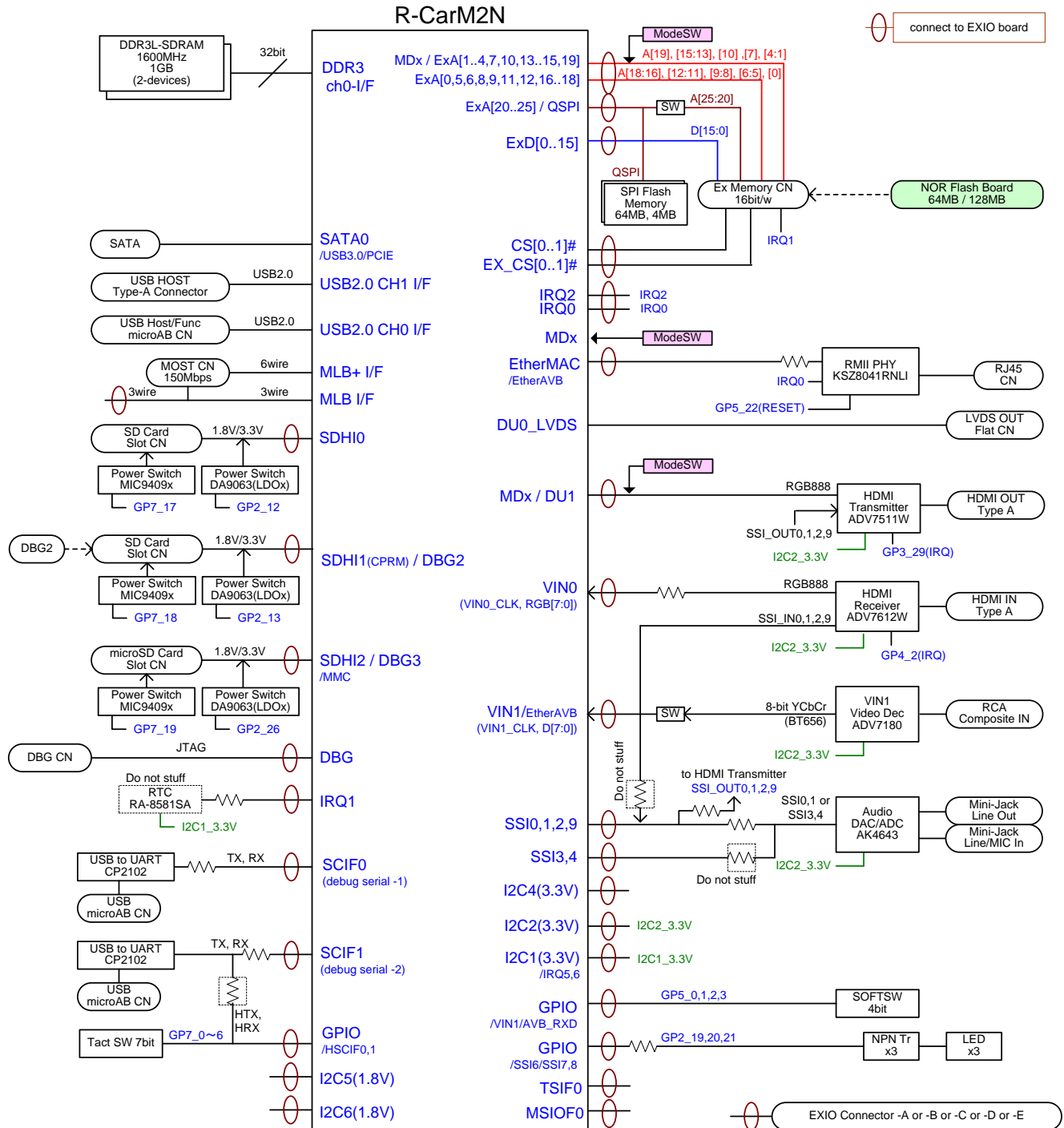


Figure 1.3.1 Block Diagram of GOSE Board

1.3.2. Address Map of GOSE Board

The address map of the LBSC space is shown below.

For the DDR3L memory space, see the section DDR3L-SDRAM Interface.

For the other space, see the R-Car Series, 2nd Generation User's Manual:Hardware.

| Area Configuration 1 | | Area Configuration 2 | | Area Configuration 3 | | Area Configuration 4 | |
|------------------------------------|-------|------------------------------------|--|-------------------------------------|-------------------------------|-------------------------------------|-------------------------------|
| [MD4=0] SW16=[2-3], SW18=ALL ON | | [MD4=1] SW16=[2-3], SW18=ALL ON | | [MD4=0] SW16=[1-2], SW18=ALL OFF | | [MD4=1] SW16=[1-2], SW18=ALL OFF | |
| AREA0 (CS0) 64MB | | H'0000_0000 | External Memory Connector CN7 64MB, 16bit/W | H'0000_0000 | Ex MEM CN CN7 1MB, 16bit/W | H'0000_0000 | Ex MEM CN CN7 1MB, 16bit/W |
| | | H'03FF_FFFF | | H'000F_FFFF | | H'000F_FFFF | |
| AREA1 (CS1) 64MB | | H'0400_0000 | External Memory Connector CN7 64MB, 16bit/W | H'0400_0000 | Ex MEM CN CN7 1MB, 16bit/W | H'0400_0000 | Ex MEM CN CN7 1MB, 16bit/W |
| | | H'07FF_FFFF | | H'040F_FFFF | | H'040F_FFFF | |
| AREA6 (0~ 64MB) | | H'0800_0000 | Other module space | H'0800_0000 | Other module space | H'0800_0000 | Other module space |
| | | H'17FF_FFFF | | H'17FF_FFFF | | H'17FF_FFFF | |
| | EXCS0 | H'1800_0000 | External Memory Connector CN7 | H'1800_0000 | External Memory Connector CN7 | H'1800_0000 | External Memory Connector CN7 |
| | EXCS1 | | | | | | |
| | EXCS2 | H'1BFF_FFFF | External Memory Connector CN7 | H'1BFF_FFFF | External Memory Connector CN7 | H'1BFF_FFFF | External Memory Connector CN7 |
| | EXCS3 | | Not available for allocation | | Not available for allocation | | Not available for allocation |
| | EXCS4 | | Not available for allocation | | Not available for allocation | | Not available for allocation |
| | EXCS5 | | Not available for allocation | | Not available for allocation | | Not available for allocation |
| | | | | | | | |
| | | | | | | | |

Figure 1.3.2 Address Map of GOSE Board

2. GOSE Interface Module Specifications

2.1. Mode Setting

2.1.1. Specifications

The operating mode of the R-CarM2N is set by a power-on reset. For details on the operating mode, see the documents related to the R-CarM2N operating mode specifications.

2.1.1.1. MD0 Pin — Selection of Free-Running Mode or Step-Up Mode

This pin selects the free-running mode or step-up mode.

| MD0 | Free-Running Mode or Step-Up Mode |
|-----|-----------------------------------|
| 0 | Free-running mode |
| 1 | Step-up mode |

2.1.1.2. MD[3:1] Pins — Selection of Boot Device

These pins select the boot device.

| MD3 | MD2 | MD1 | Selection of Boot Device |
|-----|-----|-----|--|
| 0 | 0 | 0 | Boot from area 0 (boot from the external mask ROM) |
| 0 | 1 | 0 | QSPI (48.75 MHz/16-Kbyte transfer) |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | QSPI (39 MHz/16-Kbyte transfer) |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | QSPI (39 MHz/4-Kbyte transfer) |
| 1 | 1 | 1 | Reserved |

2.1.1.3. MD4 Pin — Selection of CS0 Space Size

This pin selects whether the area 0 space (CS0) is used as a normal space (64 Mbytes) or an expanded space (128 Mbytes).

| MD4 | Area Division |
|-----|--------------------|
| 0 | Area 0: 64 Mbytes |
| 1 | Area 0: 128 Mbytes |

2.1.1.4. MD5 Pin — Selection of Secure or Non-Secure Mode

This pin selects the secure or non-secure mode

| MD5 | Selection of Secure or Non-Secure Mode |
|-----|--|
| 0 | Secure |
| 1 | Non-secure |

2.1.1.5. MD[7:6] Pins — Selection of Master Boot Processor

These pins select the master boot processor.

| MD7 | MD6 | Selection of Master Boot Processor |
|-----|-----|------------------------------------|
| 0 | 0 | CA15 boot |
| 0 | 1 | Setting prohibited |
| 1 | 0 | SH boot (32 bits) |
| 1 | 1 | Setting prohibited |

2.1.1.6. MD8 Pin — Selection of Area 0 Space Data Bus Width

This pin sets the data bus width of the area 0 space (CS0) to 8 bits or 16 bits. Select the data bus width of the boot device connected to the LBSC.

| MD8 | EXBUS Area 0 Data Bus Width |
|-----|-----------------------------|
| 0 | 8-bit bus |
| 1 | 16-bit bus |

2.1.1.7. MD9 Pin — Selection of Crystal Resonator or Crystal Oscillator

This pin selects either a crystal resonator or a crystal oscillator to be connected to the EXTAL/XTAL pins. A crystal oscillator (X6: 20 MHz) is mounted on the GOSE board by default. The crystal resonator (X5) and its peripheral circuit are not mounted.

| MD9 | EXTAL/XTAL Pin Setting |
|-----|--|
| 0 | An external clock is input to the EXTAL pin. |
| 1 | A crystal resonator is connected to the EXTAL and XTAL pins. |

2.1.1.8. MD12 — Reserved

Do not change the initial setting at shipment (MD12 = 0).

2.1.1.9. MD21, MD20, MD11, MD10, and MDT[1:0] Pins — Switching of JTAG, SDHI1, and SDHI2

These pins select the debugging function through the JTAG connector (CN1) or the SD card slot for the SDHI1 (CN9). The debugging through the SDHI1 or SDHI2 is possible by the combination of MD pin settings in the R-CarM2N specifications.

| MD10 | MD[21:20] | MD11 | MDT[1:0] | JTAG | SDHI1 | SDHI2 |
|------|-----------|------|----------|----------------------|----------------------|-----------------|
| 0 | 00 | - | -- | Boundary scan | Normal function | Normal function |
| 0 | 10 | 0 | -- | Coresight Debug Port | Normal function | Normal function |
| 0 | 10 | 1 | 00 | Coresight Debug Port | Audio DSP | Normal function |
| 0 | 10 | 1 | 01 | Coresight Debug Port | SH-4A | Normal function |
| 0 | 10 | 1 | 10 | Coresight Debug Port | Normal function | Audio DSP |
| 0 | 10 | 1 | 11 | Coresight Debug Port | Normal function | SH-4A |
| 0 | 11 | 0 | -- | SH-4A | Normal function | Normal function |
| 0 | 11 | 1 | 00 | SH-4A | Coresight Debug Port | Normal function |
| 1 | 01 | 0 | -- | Coresight Debug Port | Normal function | Normal function |
| 1 | 01 | 1 | 00 | Coresight Debug Port | GPS | Normal function |
| 1 | 01 | 1 | 01 | Coresight Debug Port | SH-4A | Normal function |
| 1 | 10 | 0 | -- | SH-4A | Normal function | Normal function |

2.1.1.10. MD[14:13] Pins — Frequency Mode Setting

These pins select the frequency mode. A crystal oscillator (X6: 20 MHz) is mounted on the GOSE board.

Do not change the initial setting at shipment (MD14 = 0, MD13 = 1).

| MD14 | MD13 | EXTAL Frequency | EXTAL Divider | PLL1 (CPGM Main) | PLL0 (CPGMC) | PLL3 DDR1600/DDR1333 MD19 = 0/MD19 = 1 |
|------|------|-----------------|---------------|------------------------|------------------------|---|
| 0 | 0 | 15 MHz | × 1/1 | ×208 VCO = 3120 MHz | ×172 VCO = 1290 MHz | ×106/×88 VCO = 1590 MHz/1320 MHz |
| 0 | 1 | 20 MHz | × 1/1 | ×156 VCO = 3120 MHz | ×130 VCO = 1300 MHz | ×80/×66 VCO = 1600 MHz/1320 MHz |
| 1 | 0 | 26 MHz | × 1/2 | ×240 VCO = 3120 MHz | ×200 VCO = 1300 MHz | ×122/×102 VCO = 1586 MHz/1326 MHz |
| 1 | 1 | 30 MHz | × 1/2 | ×208 VCO = 3120 MHz | ×172 VCO = 1290 MHz | ×106/×88 VCO = 1590 MHz/1320 MHz |

2.1.1.11. MD19 Pin — Selection of DDR3-SDRAM Bus Clock

This pin selects the frequency of the DDR3-SDRAM bus clock.

| MD19 | Switching of DDR Clock |
|------|------------------------|
| 0 | DDR3-1600 mode |
| 1 | DDR3-1333 mode |

2.1.1.12. MD28, MD27, and MD22 Pins — Selection of DDR Mode

These pins select the DDR3-SDRAM interface mode.

| MD28 | MD27 | MD22 | DDR mode | Remarks |
|------|------|------|----------------|---------|
| 1 | 1 | 0 | DDR32bit x 1ch | (Fixed) |

Note: The MD28, MD27, and MD22 pins are fixed on the board.

2.1.1.13. MD[24:23] Pins — Selection of SATA0, USB3.0, or PCIE Function

These pins select the SATA0, USB3.0, or PCIE function. MD24 and MD23 pins are fixed to “0” on the GOSE board.

| MD24 | MD23 | SATA0 / USB3.0 / PCIE |
|------|------|-----------------------|
| 0 | 0 | SATA0(fixed) |
| 0 | 1 | USB3.0 |
| 1 | 0 | PCIE |

2.1.2. Initial Values of Mode Setting Pins on GOSE Board

Table 2.1.1 Initial Values of R-CarM2N Mode Setting Pins on GOSE Board

| MD Pins | Initial Value | Initial Function |
|---------------------------------|---------------|---|
| MD0 | 0 | Free-running mode |
| MD[3:1] | 010 | Boot from QSPI |
| MD4 | 0 | CS0 space size (64 Mbytes) |
| MD5 | 1 | Non-secure mode |
| MD[7:6] | 00 | Cortex-A15 boot |
| MD8 | 1 | CS0 space data bus width (16 bits) |
| MD9 | 0 | Crystal oscillator is used. |
| MD12 | 0 | - |
| MD10, MD[21:20], MD11, MDT[1:0] | 0,00,0,00 | JTAG (CN1) = Boundary SCAN SDHI1 and SDHI2 = Normal function |
| MD[14:13] | 01 | Input frequency = 20 MHz |
| MD19 | 0 | DDR3-1600 mode |
| MD28, MD27, MD22 | 110 | DDR 32 bits × 1ch |
| MD[24:23] | 00 | SATA0 |

2.1.3. Multiplexing and Method of Setting for Mode Setting Pins

The following table covers the pin functions that are multiplexed with the mode pins of the R-CarM2N, and how the individual mode pins are set.

For the mode pins that are used with fixed values, resistors are used to set them to their fixed values according to the initial settings in table 2.1.1, Initial Values of R-CarM2N Mode Setting Pins on GOSE Board. Such mode pins are described as "Fixed by a resistor" in the Setting Method column in the table below.

Table 2.1.2 Pin Multiplexing of Mode Setting Pins of R-CarM2N

| MD Pin | Pin Function | Strapping Options | Setting Method | Default |
|--------|---------------------|-----------------------------------|---------------------|-----------------|
| MD0 | DU1_CDE (GPIO) | Free-running (0)/Step-up (1) | Set by SW9 | ON (0) |
| MD1 | DU1_DISP | Selects boot device | Set by SW9 | ON (0) |
| MD2 | DU1_VSYNC | | Set by SW9 | ON (0) |
| MD3 | DU1_HSYNC | | Set by SW9 | ON (0) |
| MD4 | WE1# | Selects area 0 size | Set by SW8 | ON (0) |
| MD5 | AUDIO_CLKOUT (GPIO) | Secure (0) or non-secure (1) mode | Set by SW10 | OFF (1) |
| MD6 | WE0# | Selects boot processor | Set by SW8 | ON (0) |
| MD7 | DACK0 (GPIO) | | Set by SW8 | ON (0) |
| MD8 | EX_CS5# (GPIO) | Selects EXBUS width | Fixed by a resistor | Pulled-up (1) |
| MD9 | EX_CS3# (GPIO) | EXTAL or EXTAL/XTAL | Fixed by a resistor | Pulled-down (0) |
| MD10 | BS# | Debugging mode | Set by SW8 | ON (0) |
| MD11 | DU1_DB5 | | Set by SW9 | ON (0) |
| MD12 | RD# | - | Set by SW8 | ON (0) |
| MD13 | A3 | Selects frequency mode | Fixed by a resistor | Pulled-up (1) |
| MD14 | A19 | | Fixed by a resistor | Pulled-down (0) |
| MD15 | - | - | - | - |
| MD16 | - | - | - | - |
| MD17 | - | - | - | - |
| MD18 | - | - | - | - |
| MD19 | A14 | DDR clock 1600/1333 | Set by SW8 | ON (0) |
| MD20 | A15 | Debugging mode | Set by SW8 | ON (0) |
| MD21 | A13 | | Set by SW8 | ON (0) |
| MD22 | A10 | DDR mode | Fixed by a resistor | Pulled-down (0) |
| MD23 | A2 | Selects SATA0/USB3.0/PCIE | Fixed by a resistor | Pulled-down (0) |
| MD24 | A4 | | Fixed by a resistor | Pulled-down (0) |
| MD25 | - | - | - | - |
| MD26 | - | - | - | - |
| MD27 | A7 | DDR mode | Fixed by a resistor | Pulled-up (1) |
| MD28 | A1 | | Fixed by a resistor | Pulled-up (1) |
| MDT0 | SIM0_CLK | Debugging mode | Set by SW10 | ON (0) |
| MDT1 | SIM0_RST | | Set by SW10 | ON (0) |

2.1.4. Block Diagram of Peripheral Circuit for Mode Pins

On the GOSE board, pull-up (100 k Ω) and pull-down (10 k Ω) resistors are used to implement the settings of the mode pins that are largely used with fixed values. When changes to the settings of mode pins are likely, this can be implemented by switches which, through resistive voltage division, select the low level when turned on and the high level when turned off.

When the R-CarM2N is released from the power-on reset (when the PRESET# signal of the R-CarM2N is changed from low to high), the mode value set by the switch or resistive voltage division is input to the R-CarM2N.

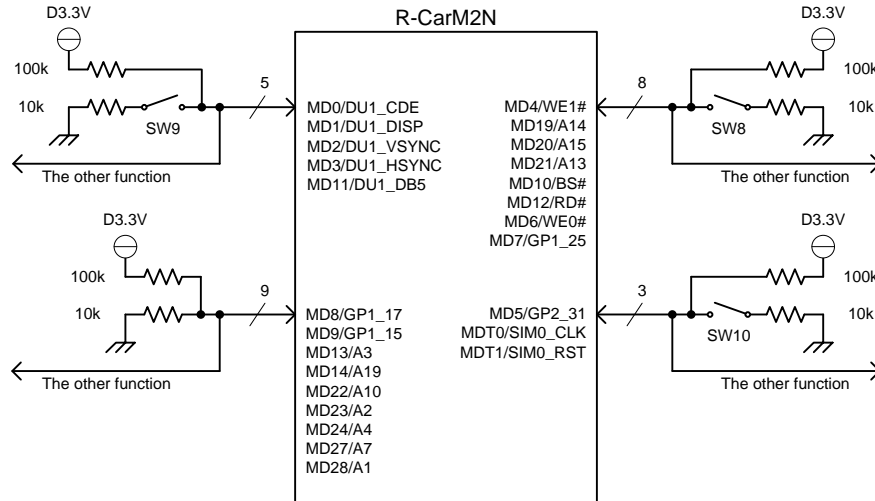


Figure 2.1.1 Peripheral Circuit for Mode Pins on GOSE Board

2.2. DDR3L-SDRAM Interface

2.2.1. Specifications

The GOSE board incorporates two 4-Gbit DDR3L-SDRAMs (16-bit bus width) (DDR: 32 bits × 1 channels) and operates at a maximum speed of DDR3-1600. On the GOSE board, the R-CarM2N and DDR3L-SDRAMs are connected in 32-bit × 1-channel mode; the DDR3L-SDRAMs are allocated to the address space from H'01_0000 0000 to H'01_3FFF FFFF. The address ranges from H'00_4000 0000 to H'00_7FFF FFFF can be accessed by default as a mirror area of H'01_0000 0000 to H'01_3FFF FFFF.

Table 2.2.1 DDR3L-SDRAM Specifications

| | |
|---------------------------------------|--|
| Interface | DDR3L-SDRAM |
| Product name | MT41K256M16HA-125 AIT:E (DDR3-1600, ×16 bits, 4 Gbits) × 2 pcs |
| Power supply voltage | 1.35 V |
| Capacity | Total: 1 Gbytes, H'01_0000 0000 to H'01_3FFF FFFF |
| Bus width | 32-bit data bus × 1ch |
| Memory bus frequency (R-CarM2N spec.) | DDR3-1600 max. |

2.2.2. Signal Correlation

Table 2.2.2 DDR3L-SDRAM Signal Correlation

| R-CarM2N (DDR32bit x 1ch) | DDR3L-SDRAM | |
|------------------------------|--------------------------|--------------------------|
| | Channel 0 | |
| | M3 | M4 |
| | D[31:16] | D[15:0] |
| M0DQ[31:16] | DQU[7:0],DQL[7:0] | - |
| M0DQ[15:0] | - | DQU[7:0],DQL[7:0] |
| M0A[15:0] | A[15:0] | A[15:0] |
| M0BA[2:0] | BA[2:0] | BA[2:0] |
| M0CK1,M0CK1# | CK, CK# | - |
| M0CK0,M0CK0# | - | CK, CK# |
| M0CKE1 | CKE | - |
| M0CKE0 | - | CKE |
| M0CS1# | CS# | - |
| M0CS0# | - | CS# |
| M0WE# | WE# | WE# |
| M0RAS# | RAS# | RAS# |
| M0CAS# | CAS# | CAS# |
| M0DQS[3:2], M0DQS[3:2]# | DQSU,DQSL DQSU#,DQSL# | - |
| M0DQS[1:0] M0DQS[1:0]# | - | DQSU,DQSL DQSU#,DQSL# |
| M0DM[3:2] | DMU,DML | - |
| M0DM[1:0] | - | DMU,DML |
| M0ODT1 | ODT | - |
| M0ODT0 | - | ODT |
| M0RESET# | RESET# | RESET# |

(*) Half voltage of VDDQ_M0 is supplied to the M0VREFDQ[1:0] pins of the R-CarM2N.

2.2.3. Block Diagram

The following figure shows a block diagram of the DDR3L-SDRAM interface.

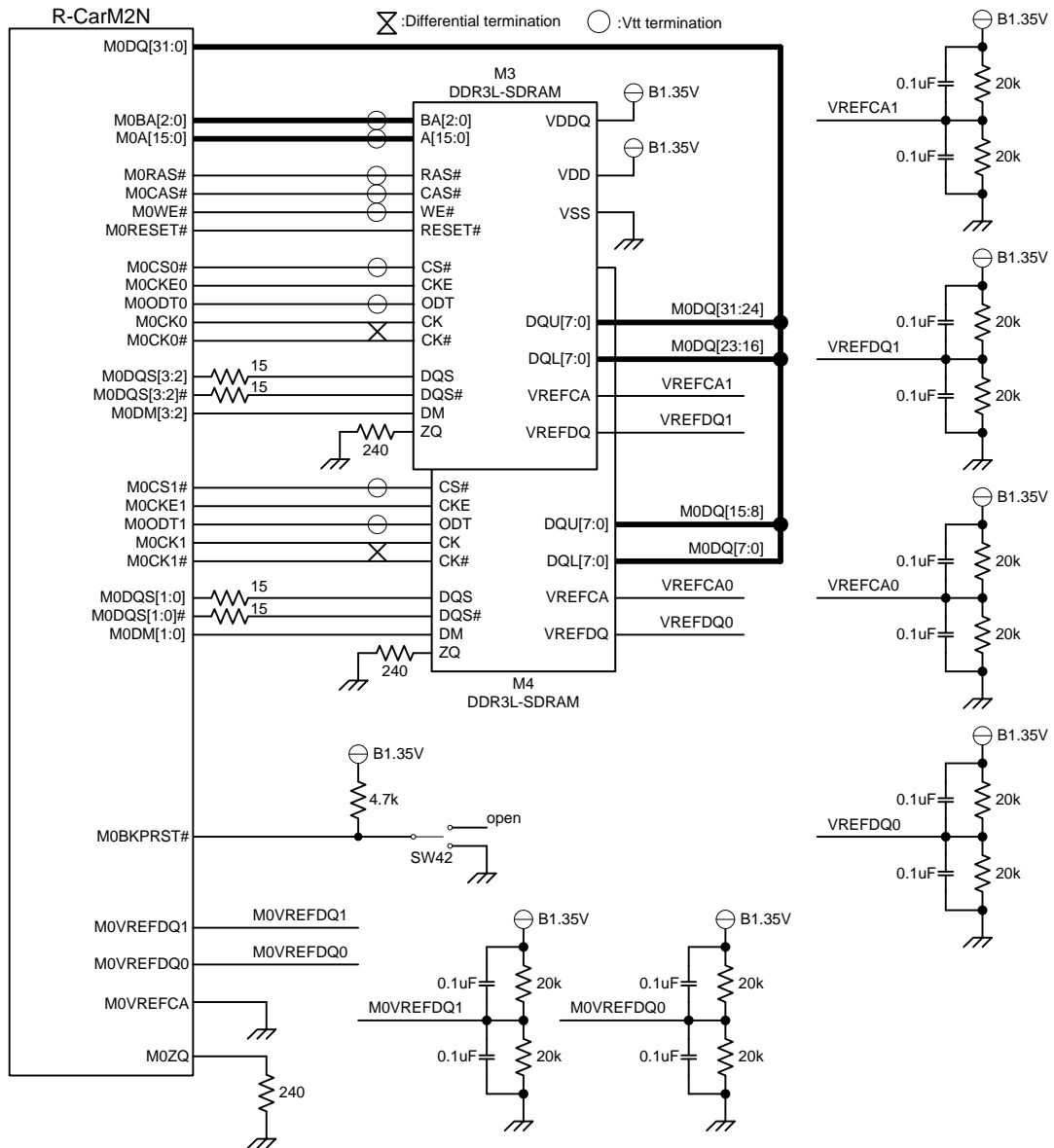


Figure 2.2.1 Block Diagram of DDR3L-SDRAM Interface

2.3. Flash Memory Sub-Board Interface

2.3.1. Specifications

The GOSE board has a connector (CN7) to connect a flash memory sub-board. R0P0400C0001FS can be connected as a flash memory sub-board. The specifications of R0P0400C0001FS are summarized in the table below.

The R0P0400C0001FS board incorporates two flash memory devices S29GL512N10TFIR10 (512 Mbits × 16 bits).

The capacity can be set to 64 Mbytes or 128 Mbytes by the switch settings on the flash memory sub-board. The flash memory sub-board is connected to the R-CarM2N via a 16-bit data bus and can be mapped to area 0 (CS0) or area 1 (CS1). For details, see the specifications of R0P0400C0001FS.

Area 0 (CS0) can be used as a 128-Mbyte space by setting the capacity of the flash memory sub-board to 128 Mbytes and pin 1 of SW8 (MD4) to off.

Note:

The QSPI pins are multiplexed with the higher-order address pins (A20 to A25) of the LBSC due to the specifications of the R-CarM2N's pin function controller. Accordingly, when the QSPI is in use, only the lower-order address pins (A0 to A19) of the LBSC are available for use.

Note:

When R0P0400C0001FS is used on the GOSE board, settings of SW16 and SW18 are required. Set SW16 and SW18 as follows depending on the capacity.

[A] When used with the capacity of 64 Mbytes (128 Mbytes) (i.e., the QSPI is not in use)

Set SW16 to the pin 3 side and set SW18 to all on.

[B] When used with the capacity of 1 Mbyte (A0 to A19) (i.e., the QSPI is in use)

Set SW16 to pin 1 side and set SW18 to all off.

Note:

When R0P0400C0001FS is used on the GOSE board, it cannot be used in 32-bit data bus width mode since the R-CarM2N only supports data bus width of 16 bits.

Note:

Do not connect other types of flash memory board such as FMRS6401 to the GOSE board since it does not support access to them.

Table 2.3.1 Flash Memory Sub-Board Specifications

| | |
|-------------------|---|
| Flash sub-board | R0P0400C0001FS (Renesas Electronics original board) |
| Flash memory | S29GL512N10TFIR10 (512 Mbits, 8-/16-bit data width configuration) by Spansion × 2 pcs |
| Operating voltage | 3.3 V |
| Capacity | 64 Mbytes or 128 Mbytes (selectable) |
| Mapping area | Area 0 or area 1 (selectable) |
| Bus width | Only 16-bit data bus width on the GOSE board |
| Connector | 'CN7' on the GOSE board |

For details on the flash memory board, refer to the related documents.

2.3.2. Block Diagram

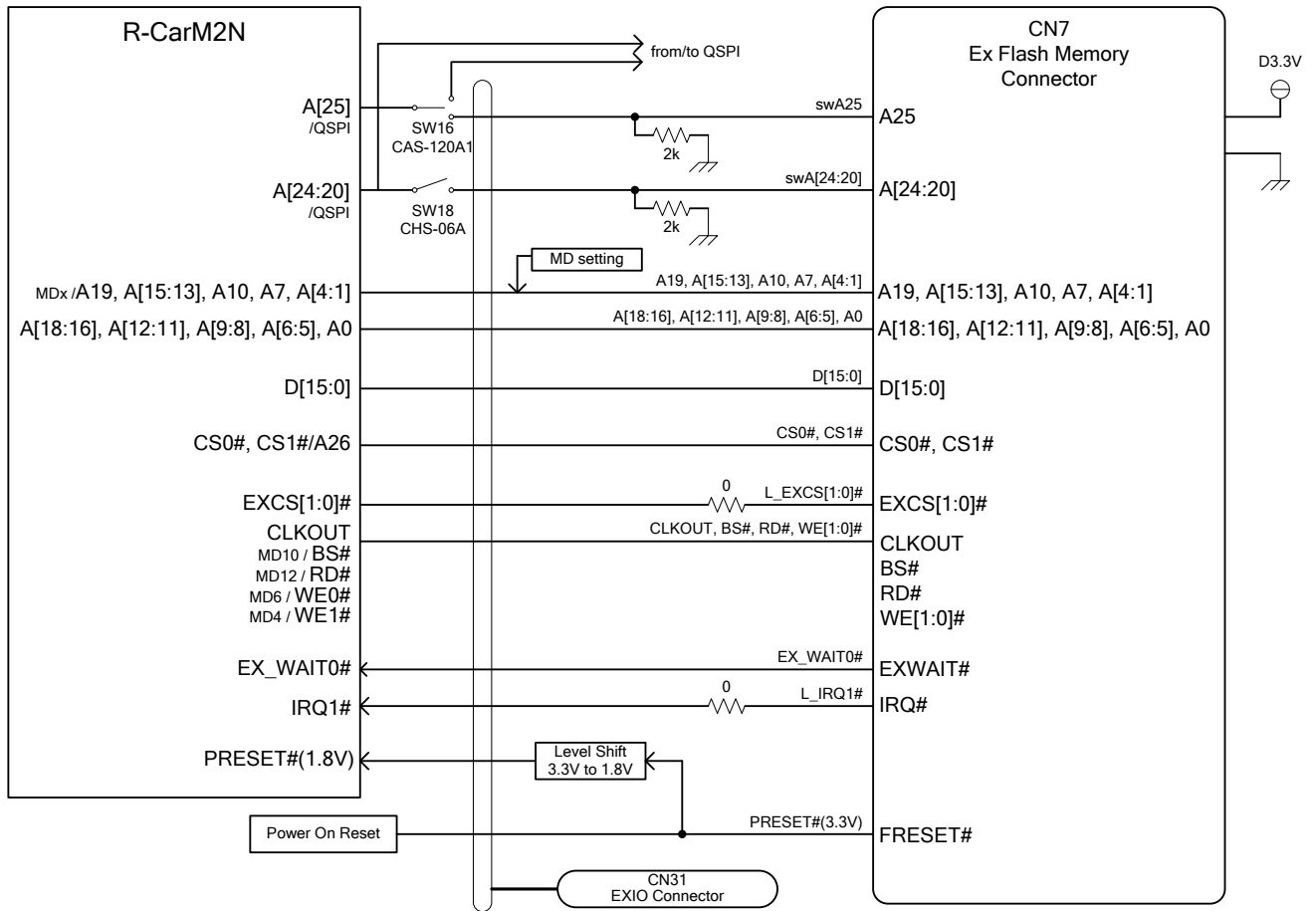


Figure 2.3.1 Block Diagram of Flash Memory Sub-Board Interface

2.4. SPI-Flash Interface (QSPI)

2.4.1. Specifications

The GOSE board incorporates 512-Mbit and 32-Mbit SPI flash memory devices manufactured by Spansion. These SPI flash memory devices are connected to the QSPI of the R-CarM2N via switches SW16 and SW17. By setting SW9, booting from the QSPI is possible. When the QSPI is to be used, set all SW18 switches to off. Additionally, set SW16 to the pin 1 side. When the 512-Mbit SPI flash memory (U16) is to be accessed, set SW17 to pin 1 side, and when the 32-Mbit SPI flash memory (U17) is to be accessed, set SW17 to the pin 3 side.

The QSPI pins are multiplexed with the higher-order address pins (A20 to A25) of the LBSC due to the specifications of the R-CarM2N's pin function controller. Accordingly, when the QSPI is in use, only the lower-order address pins (A0 to A19) of the LBSC are available for use.

Since the loader and mini-monitor are stored in the lower-order address space of the SPI flash memory (U17, 32 Mbits), do not modify the contents of this area. The contents of the SPI flash memory (U16, 512 Mbits) can be modified as required.

Table 2.4.1 SPI-FLASH Interface Specifications

| | |
|-------------------------------|---|
| QSPI controller | R-CarM2N's on-chip QSPI module |
| SPI-FLASH | (1) U16: S25FL512SAGMFIG11 by Spansion (512 Mbits) (2) U17: S25FL032P0XMF1011 by Spansion (32 Mbits) |
| Clock rate of R-CarM2N's QSPI | 48.75-MHz operation (max.) |

2.4.2. Block Diagram

A block diagram of the SPI flash memory interface is shown below.

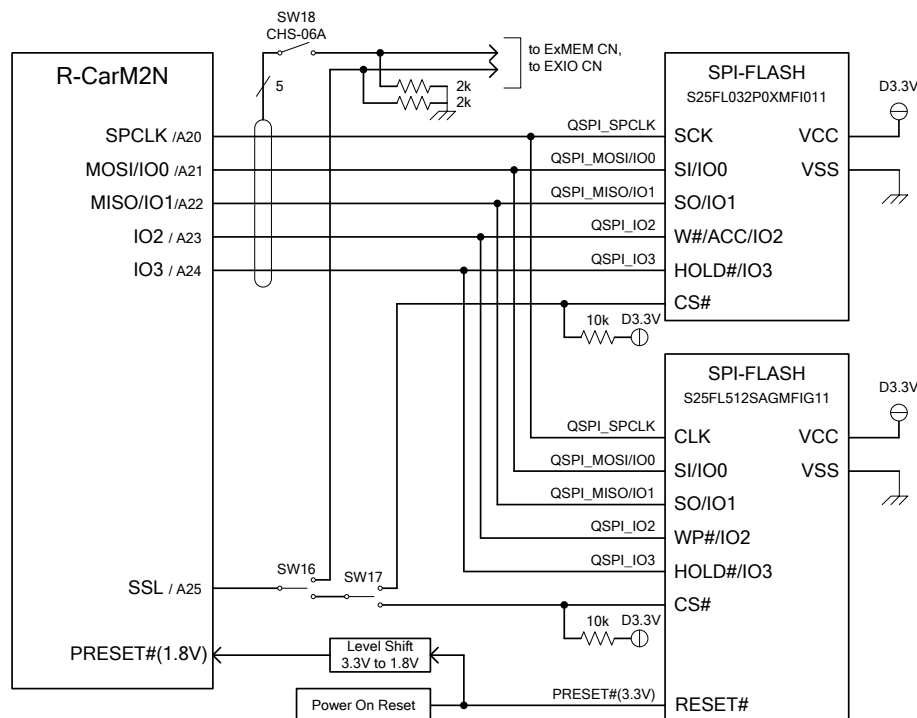


Figure 2.4.1 Block Diagram of SPI-Flash Interface

2.5. Video Input Interface

2.5.1. Specifications

The R-CarM2N has two channels of video input functions (VIN0, VIN1). For details, see the section on video input in the R-Car Series, 2nd Generation User's Manual:Hardware.

On the GOSE board, ADV7612WBSWZ (U29) manufactured by Analog Devices is connected to VIN0 of the R-CarM2N and used as an HDMI receiver. ADV7180WBCP32Z (U30) manufactured by Analog Devices is connected via switches SW23 and SW24 to VIN1 of the R-CarM2N and used as a composite video decoder. For details on the ADV7612 and ADV7180, see the datasheet of each device.

The registers of ADV7612 and ADV7180 should be set via channel 2 of the I²C.

In addition, all signals of the video input interface are connected to EXIO connector D (CN34).

Note:

HDMI input of GOSE does not support interlace mode. GOSE supports only progressive mode.

Table 2.5.1 Video Input Specifications

| | |
|----------------------------------|--|
| Video input module | R-CarM2N's on-chip video input module channels 0 and 1 |
| HDMI receiver for VIN0 | U29: ADV7612WBSWZ by Analog Devices I ² C-BUS ch2 slave address = H'98 for write, H'99 for read (ALSB = 0) |
| Composite video decoder for VIN1 | U30: ADV7180WBCP32Z by Analog Devices I ² C-BUS ch2 slave address = H'40 for write, H'41 for read |
| Video input connector | CN15: Type A HDMI connector for VIN0 CN16: RCA connector for VIN1 |

2.5.2. Block Diagram

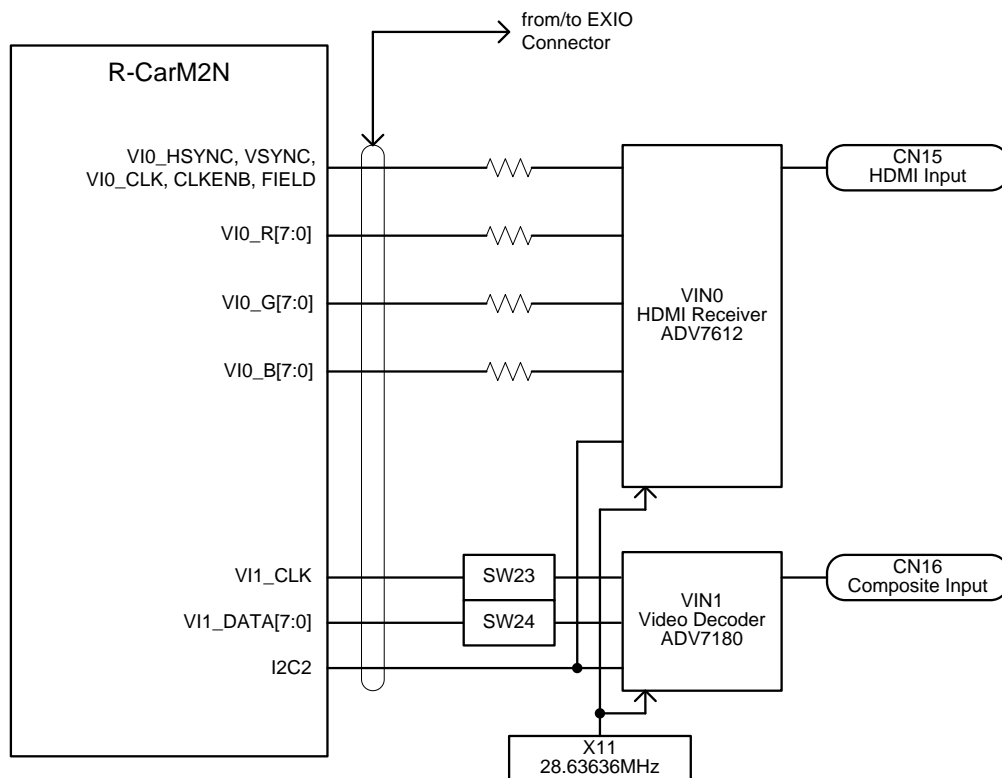


Figure 2.5.1 Block Diagram of Video Input Interface

2.6. Video Input Interface 0

2.6.1. Specifications

On the GOSE board, ADV7612WBSWZ (U29) manufactured by Analog Devices is connected to VIN0 of the R-CarM2N and used as an HDMI receiver. The ADV7612WBSWZ (U29) handles inputs in the RGB888, RGB666, Y[7:0]/CbCr[7:0], and YCbCr[7:0] formats. The block diagram of the VIN0 interface is shown below.

2.6.2. Block Diagram

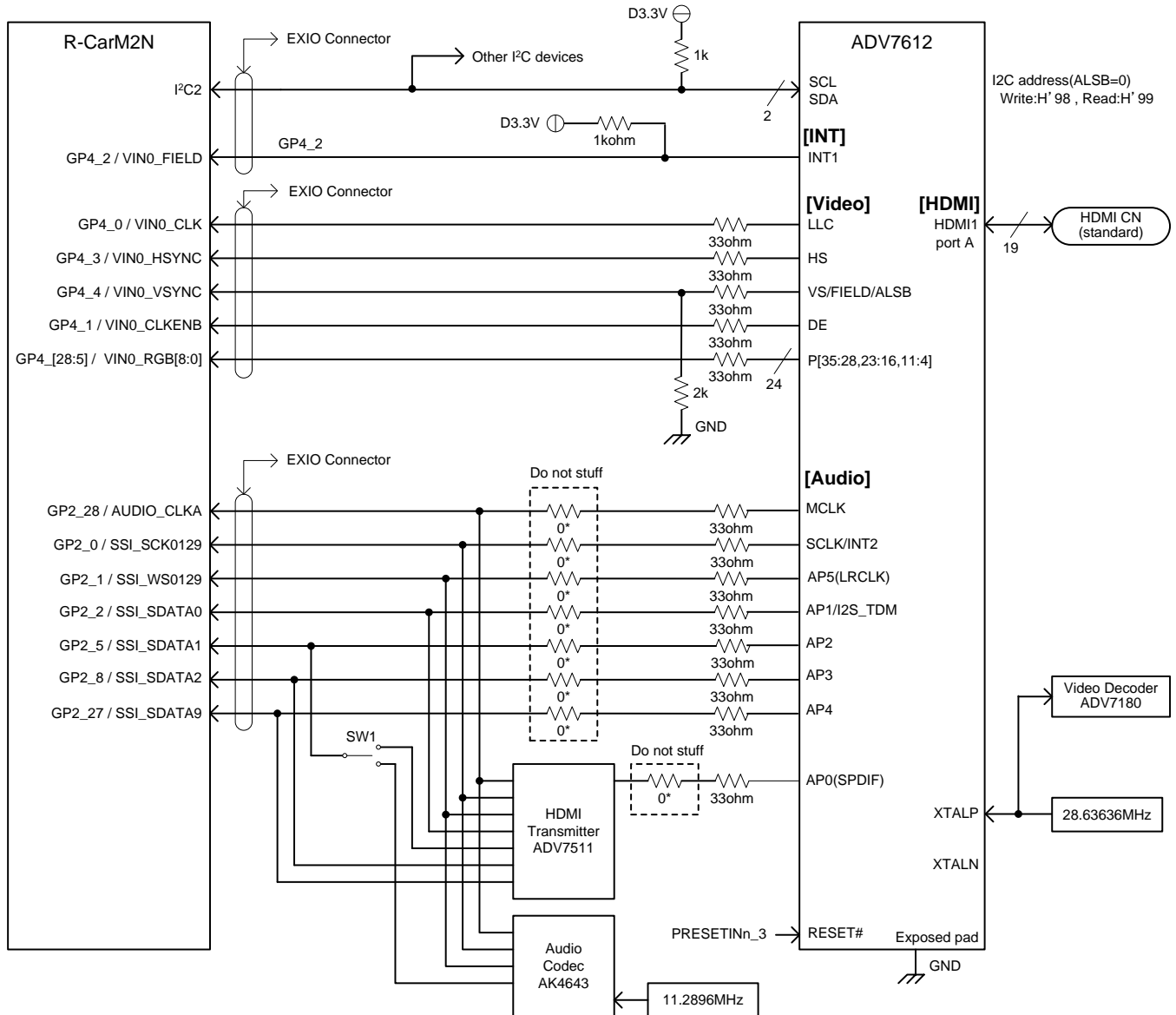


Figure 2.6.1 Block Diagram of Video Input Interface 0

2.7. Video Input Interface 1

2.7.1. Specifications

On the GOSE board, ADV7180WBCP32Z (U30) manufactured by Analog Devices is connected via switches SW23 and SW24 to VIN1 of the R-CarM2N and used as a composite video decoder. The ADV7180WBCP32Z (U30) handles inputs in the ITU-R BT.656 8-bit (YCbCr) format according to the switch settings. The block diagram of the VIN1 interface is shown below.

2.7.2. Block Diagram

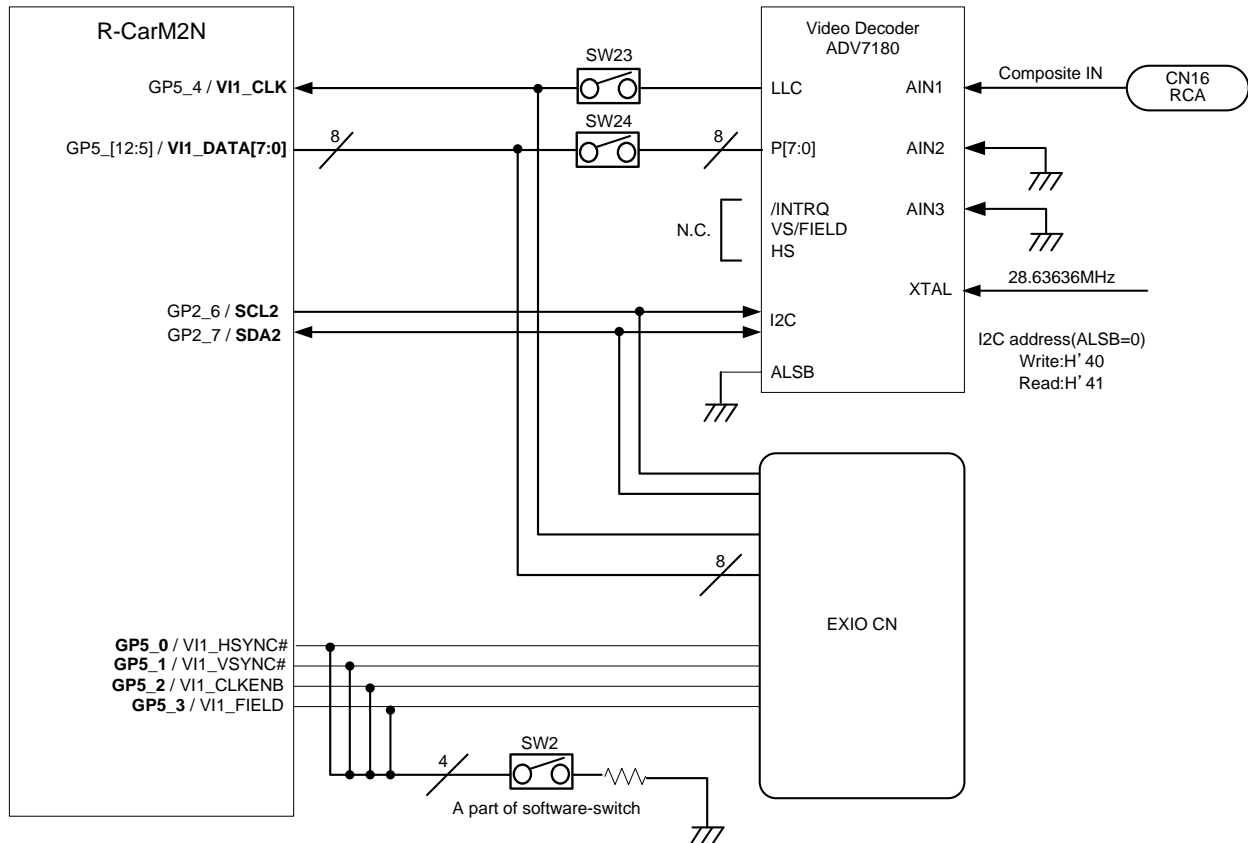


Figure 2.7.1 Block Diagram of Video Input Interface 1

2.8. Video Output Interface

2.8.1. Specifications

R-CarM2N incorporates one display unit (DU) with the LVDS interface and one display unit with the digital RGB interface.

On the GOSE board, the HDMI transmitter (ADV7511) converts the digital RGB signals of DU1 to HDMI signals. These digital RGB signals are also connected to the EXIO connector (CN30).

In addition, the LCD connector (CN13) is directly connected to DU_LVDS channel 0 (DU0_LVDS). The GOSE board also incorporates a 12-V power supply connector (CN14) and a variable resistor (VR1), respectively for power supply to the LCD backlight and brightness adjustment.

On the GOSE board, the external dot clock inputs are connected as follows: DU0_DOTCLKIN is connected to X13 (148.50 MHz) and DU1_DOTCLKIN is connected to X2 (74.25 MHz, socket-mounted). DU1_DOTCLKIN is further connected to the EXIO connector (CN30). Alternatively, a clock signal derived by frequency-dividing the R-CarM2N's internal clock can be selected. For details, see the display unit specifications in the R-Car Series, 2nd Generation User's Manual:Hardware.

Table 2.8.1 Video Output Interface Specifications

| | |
|--------------------|---|
| Display controller | R-CarM2N's on-chip display unit |
| | [LVDS Output] |
| DU0_LVDS | Connector CN13: DF14A-20P-1.25H by Hirose, for LVDS signals. CN14: SM14B-SRSS-TB(LF)(SN) by JST, for power supply of backlight. |
| | [HDMI Output] |
| | HDMI transmitter converts digital RGB signals to HDMI signals. U23: ADV7511WBSWZ by Analog Devices |
| DU1 (digital RGB) | Connector CN11: 1747981-1 (HDMI type A, standard, 19-pin) by Tyco Electronics |
| | [Digital RGB Output] |
| | Connector CN30: QSE-020-01-F-D-A by Samtec |

2.8.2. Block Diagram

A block diagram of the video output interface on the GOSE board is shown below.

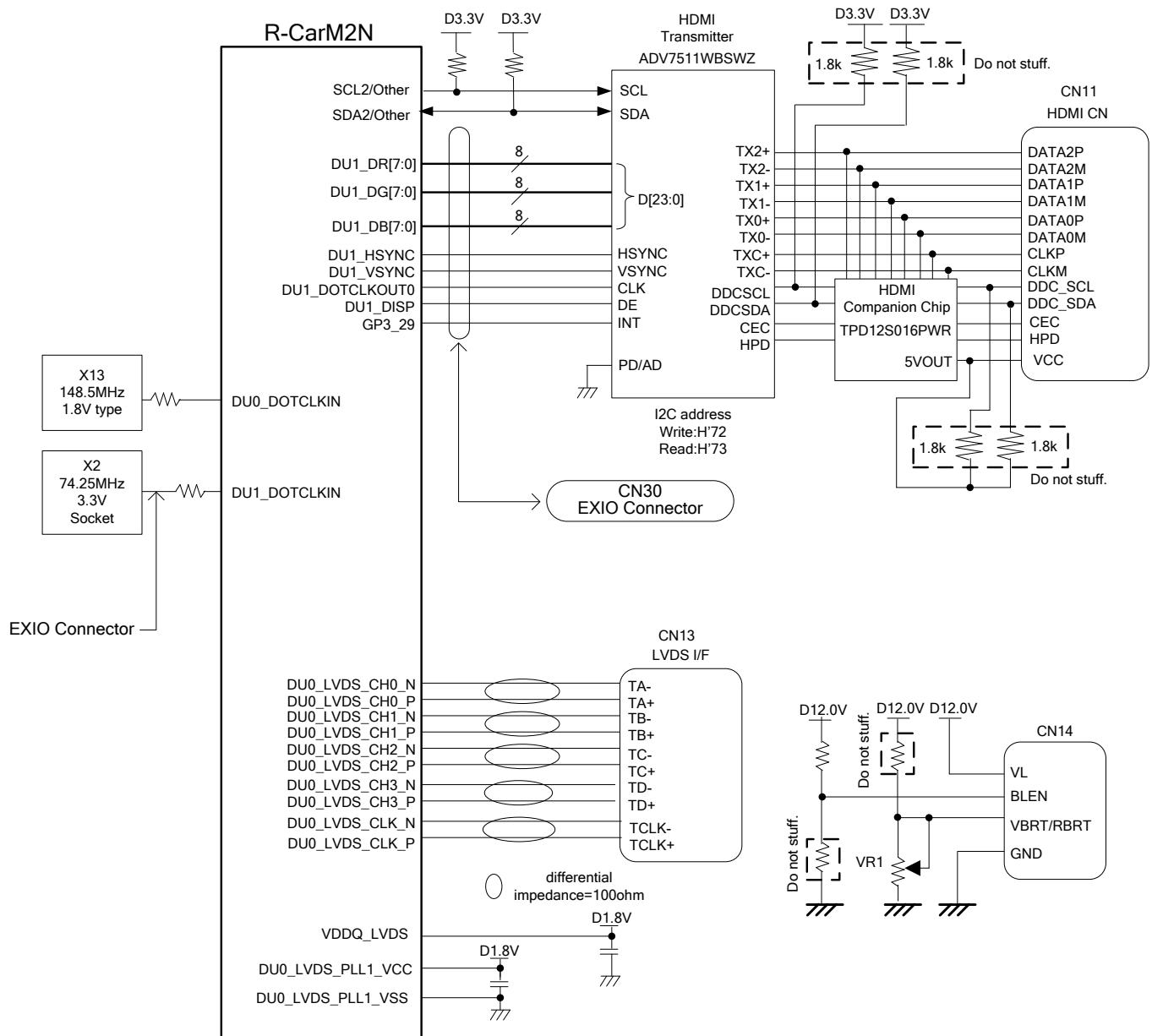


Figure 2.8.1 Block Diagram of Video Output Interface

2.9. MediaLB 6-pin/3-pin Interface

2.9.1. Specifications

The R-CarM2N incorporates a MediaLB (Media Local Bus: 6-pin differential interface) supporting the MOST150 specifications and a MediaLB (Media Local Bus: 3-pin interface) supporting the MOST50 specifications. On the GOSE board, the MediaLB pins compliant with MOST150 are assigned to a connector manufactured by Samtec, Inc. and the MediaLB pins compliant with MOST50 are assigned to the pins described as (not used) in the table below. The MediaLB compliant with the MOST150 specifications supports an INIC board (OS81110: Board variant 1) manufactured by SMSC, which has six pins for differential input and output.

The list of pins of the 40-pin connector on the GOSE board is shown below.

Table 2.9.1 MediaLB Connector Pin List

| Pin | Name | Pin | Name |
|-----|-----------------------|-----|-------------------------------|
| 1 | MLBSN | 2 | MLBCLK (not used) |
| 3 | MLBSP | 4 | Brd_ID0 (not used) |
| 5 | Brd_ID4 (not used) | 6 | MLBSIG (not used) |
| 7 | Brd_ID3 (not used) | 8 | Brd_ID1 (not used) |
| 9 | MLBDN | 10 | MLBDAT (not used) |
| 11 | MLBDP | 12 | Brd_ID2 (not used) |
| 13 | RESERVED (not used) | 14 | TVAL0/SRX1/SINTA_B (not used) |
| 15 | RESERVED (not used) | 16 | RMCK1/SRX2/SDINA (not used) |
| 17 | MLBCN | 18 | TDAT0/SRX0/SDOUTA (not used) |
| 19 | MLBCP | 20 | SRX3/SDINB (not used) |
| 21 | PS0 (not used) | 22 | PS1 (not used) |
| 23 | STATUS (not used) | 24 | PWROFF (not used) |
| 25 | RST_B | 26 | RSOUT_B (not used) |
| 27 | ERR/BOOT_B (not used) | 28 | MCK (not used) |
| 29 | TCK/DSCL (not used) | 30 | TMS (not used) |
| 31 | TDO/DINT (not used) | 32 | TDI/DSDA (not used) |
| 33 | SCL | 34 | INT_B (not used) |
| 35 | SDA | 36 | RESERVED (not used) |
| 37 | 3.3V SW | 38 | 3.3VCONT |
| 39 | 3.3V SW | 40 | 12VCONT (not used) |

Table 2.9.2 MediaLB Connector Specification

| | |
|-------------------|--------------------------------------|
| MediaLB connector | QSH-020-01-L-D-DP-A by Samtec (CN18) |
|-------------------|--------------------------------------|

2.9.2. Block Diagram

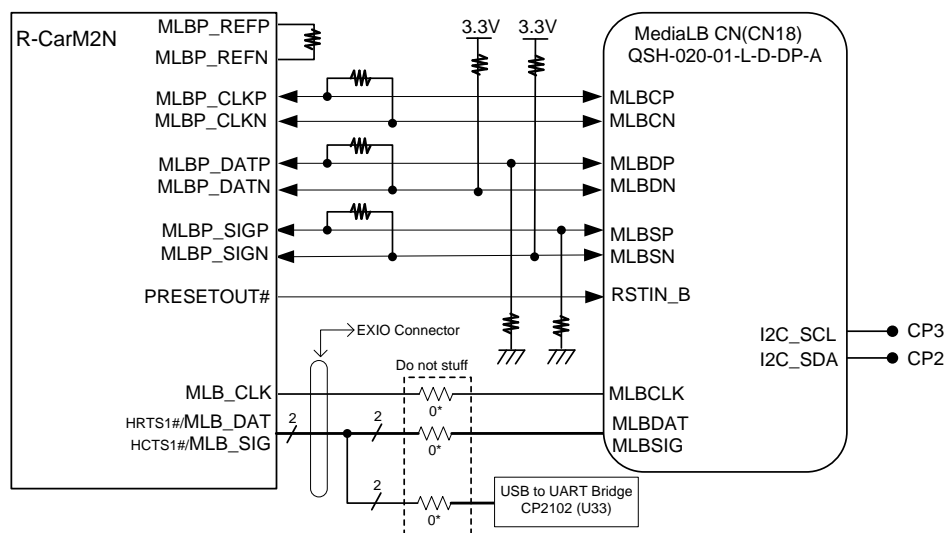


Figure 2.9.1 Block Diagram of MediaLB Interface

2.10. Debugger Interface

2.10.1. Specifications

The GOSE board incorporates two debugger interfaces; one is a 20-pin connector (DBG) for connection to the JTAG emulator and the other is an SD card slot for SDHI1 (DBG2) for connection to the debug board.

When the DBG2 interface is to be used, switch JP3 and SW20 for the use of DBG2 rather than SDHI1 and switch SW21 to “ON” to set the power supply voltage for the VCCQ_SD1 to 1.8 V.

The R-CarM2N supports the DBG3 interface as a debugger interface, but the GOSE board does not include this function. The signals related to DBG3 (SDHI1) are instead connected to EXIO connector C.

On the GOSE board, the debugging function can be selected through the JTAG connector (CN1) or the SD card slot (CN9) by settings of the mode pins. For setting of mode pins, see section 2.1.1.9, Switching of JTAG, SDHI1, and SDHI2. For details on the debugger interface, see the R-Car Series, 2nd Generation User’s Manual:Hardware.

Table 2.10.1 DBG Specifications

| | |
|-------------------------------|---|
| DBG interface (20-pin) | CN1: HTST-110-01-S-V by Samtec |
| DBG2 interface (SD card slot) | CN9: DM1AA-SF-PEJ (full SD card slot) by Hirose |

2.10.2. Block Diagram

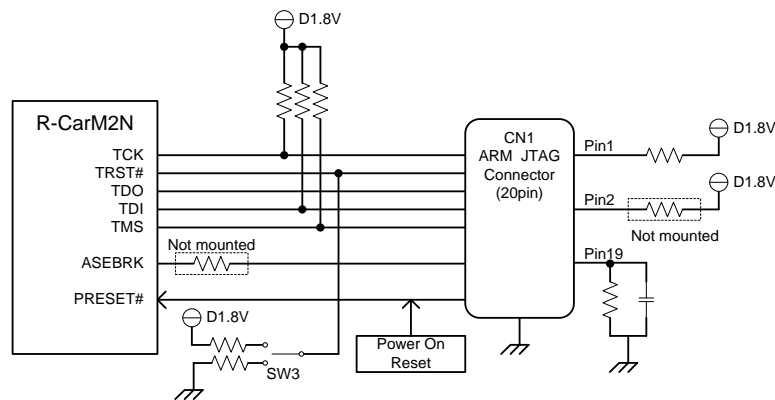


Figure 2.10.1 Block Diagram of JTAG (DBG) Interface

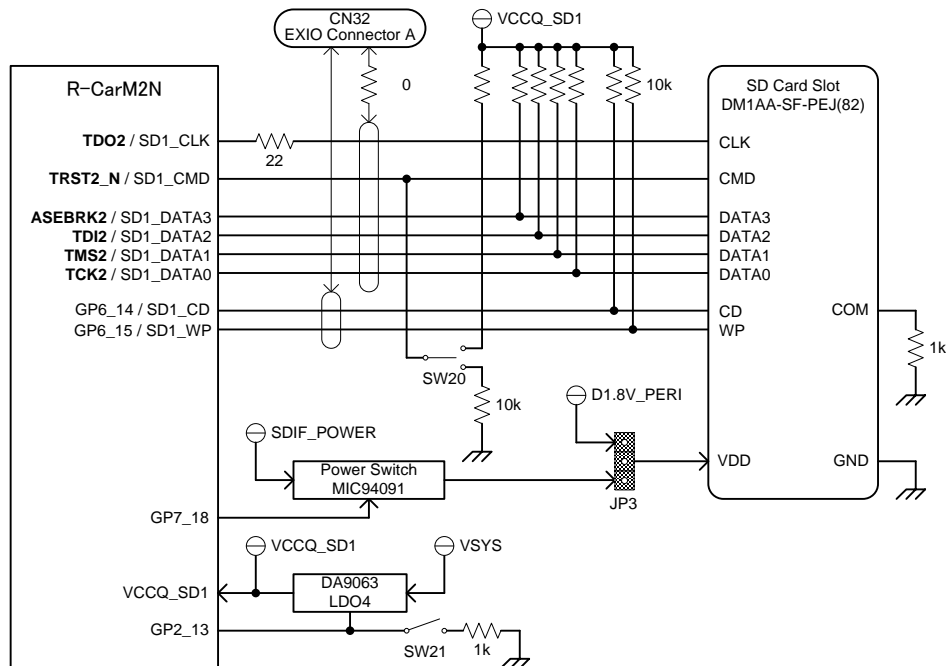


Figure 2.10.2 Block Diagram of SDHI1 Slot Debugger (DBG2) Interface

2.11. Debug Ether Interface (EtherMAC)

2.11.1. Specifications

The R-CarM2N incorporates the EtherMAC that supports 100Base-TX or 10Base-T compliant with IEEE 802.3u. On the GOSE board, the EtherMAC signals are connected to the RMII PHY interface (KSZ8041RNLI) manufactured by Micrel.

Table 2.11.1 Debug Ether Interface Specifications

| | |
|----------------------------|--|
| MAC layer | R-CarM2N's on-chip EtherMAC |
| Physical layer transceiver | U21: KSZ8041RNLI (RMII) by Micrel |
| Modular connector | CN10: TLA-6T776F (RJ-45 with pulse transformer) by TDK |

2.11.2. Block Diagram

A block diagram of the debug Ether interface is shown below.

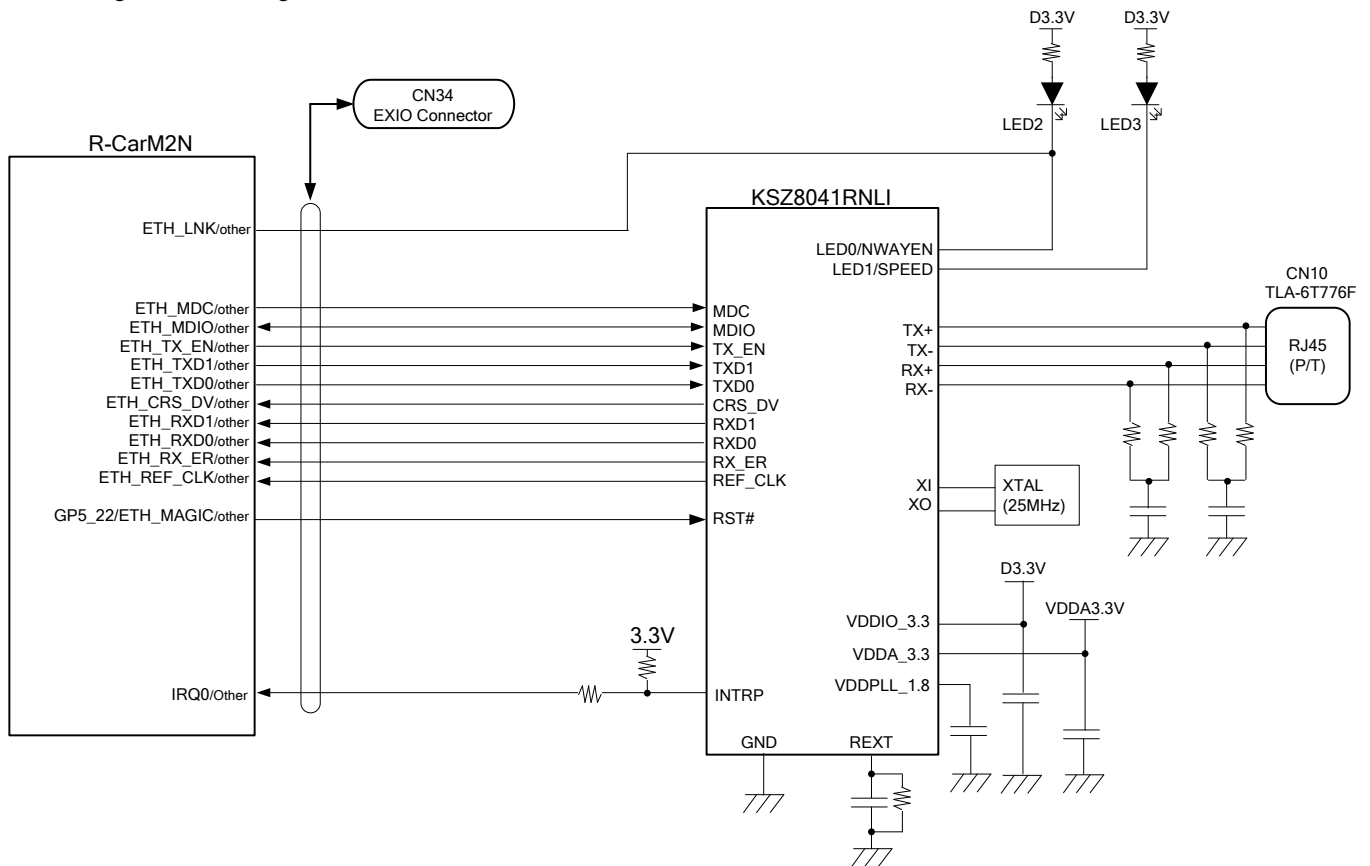


Figure 2.11.1 Block Diagram of Debug Ether Interface

2.12. Audio Codec Interface (SSI0, SSI1, SSI2, and SSI9, or SSI3 and SSI4)

2.12.1. Specifications

On the GOSE board, the codec (AK4643EN) is connected to the SSI0, SSI1, SSI3, and SSI4 of the R-CarM2N. Either SSI0 and SSI1 or SSI3 and SSI4 can be used exclusively and should be selected through 0-Ω resistors.

The PDN (power-down) pin of AK4643EN is controlled by the PRESETOUT# signal output from the R-CarM2N.

The audio interface of AK4643EN is in the slave mode after PRESETOUT# is released from a reset and can be switched to the master mode by a register that is accessed via channel 2 of the I²C. Furthermore, the SSI on the R-CarM2N side can be set as the master or a slave. It is assumed that SSI_SDATA0 or SSI_SDATA3 is set to transmit mode and SSI_SDATA1 or SSI_SDATA4 is set to receive mode on the GOSE board.

Among the signals of the audio interface, the signals of SSI0, SSI1, SSI2, and SSI9 are also connected to HDMI transmitter ADV7511 (U23), HDMI receiver ADV7612 (U29), and EXIO connector (CN32) on the GOSE board. For the connections between the R-CarM2N and each device, see table 2.12.2.

Table 2.12.1 SSI Codec Specifications

| | |
|-----------------|---|
| Controller | R-CarM2N's on-chip SSI0 and SSI1 or SSI3 and SSI4 |
| Codec | U31: AK4643EN by Asahi Kasei |
| Audio interface | R-CarM2N (SSI) = Master or slave selectable AK4643EN = Master or slave selectable (default: slave) |
| Audio connector | LINE-OUT (CN17, lower-side, 3.5-mm mini-jack) LINE-IN/MIC-IN (CN17, upper-side, 3.5-mm mini-jack) |

2.12.2. Block Diagram

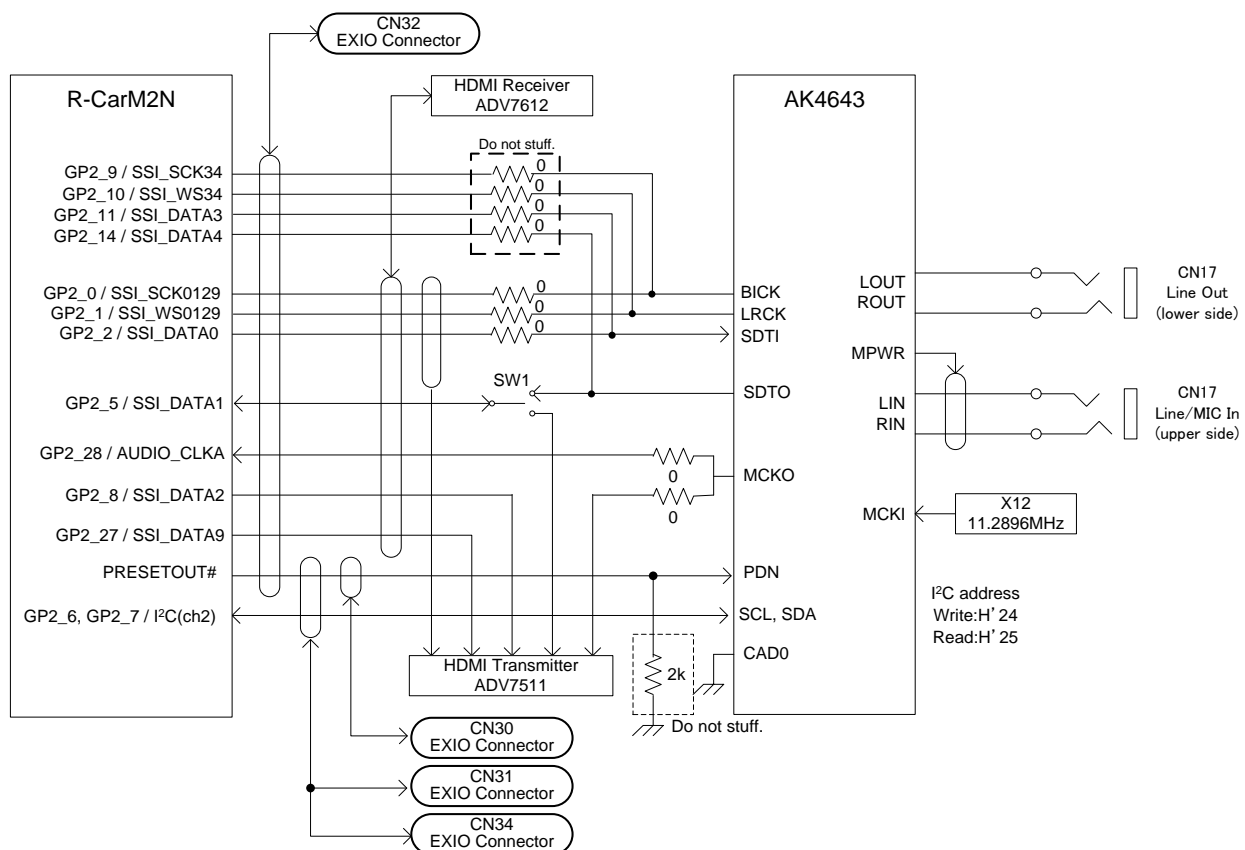


Figure 2.12.1 Block Diagram of Audio Codec Interface

Table 2.12.2 SSI Connections on the GOSE Board

| R-CarM2N | | AK4643 | ADV7511 | ADV7612 | EXIO CN (CN32) |
|----------|-------------|--|--|--|----------------|
| GP2_28 | AUDIO_CLKA | Connected. (0-Ω resistors are mounted.) | Connected. (0-Ω resistors are mounted.) | Not connected. (0-Ω resistors are NOT mounted.) | Connected. |
| GP2_0 | SSI_SCK0129 | | | | |
| GP2_1 | SSI_WS0129 | | | | |
| GP2_2 | SSI_SDATA0 | | | | |
| GP2_5 | SSI_SDATA1 | Connected. (SW1) | Connected. (SW1) | | |
| GP2_8 | SSI_SDATA2 | - | Connected. | | |
| GP2_27 | SSI_SDATA9 | - | (0-Ω resistors are mounted.) | | |
| GP2_9 | SSI_SCK34 | Not connected. (0-Ω resistors are NOT mounted.) | Not connected. | Not connected. | Connected. |
| GP2_10 | SSI_WS34 | | | | |
| GP2_11 | SSI_SDATA3 | | | | |
| GP2_14 | SSI_SDATA4 | | | | |

2.13. Serial-ATA Interface

2.13.1. Specifications

The GOSE board incorporates one serial-ATA interface (SATA0) channel. The R-CarM2N's on-chip serial-ATA interface conforms to the Serial ATA standard rev. 3.1 and supports transfer rates of 1.5 Gbps (Gen1) and 3.0 Gbps (Gen2).

The GOSE board incorporates a 4-pin power connector (CN2) for the ATAPI device. The power connector conversion cable (4-pin to 15-pin) is required to supply power to the SATA device.

Table 2.13.1 Serial-ATA Interface Specifications

| | |
|---------------------------------|--|
| Serial-ATA interface controller | R-CarM2N's on-chip serial-ATA controller |
| Serial-ATA connector (signal) | 67491-0020 by Molex (CN3) |
| Serial-ATA connector (power) | LC-04A by JST (CN2) |
| Serial-ATA clock source | IDT5V41066PGGI by IDT |

2.13.2. Block Diagram

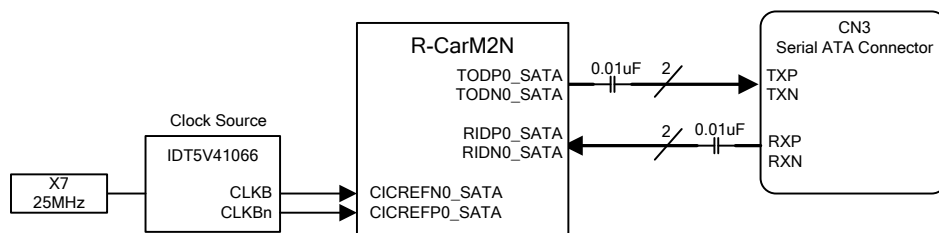


Figure 2.13.1 Block Diagram of Serial-ATA Interface

2.13.3. Serial-ATA Clock Source Unit

The details on the clock source unit of the Serial-ATA interface is shown below.

IDT5V41066PGGI manufactured by IDT is used for the clock driver. This clock driver multiplies the input frequency (25 MHz) to supply a 100-MHz differential clock to the R-CarM2N.

Note:

To reduce the difference in wiring length between each pair of differential signals from the R-CarM2N to the clock source, the P and N lines from the clock pins (CICREFP0_SATA and CICREFN0_SATA signals) are swapped before connection to the clock source.

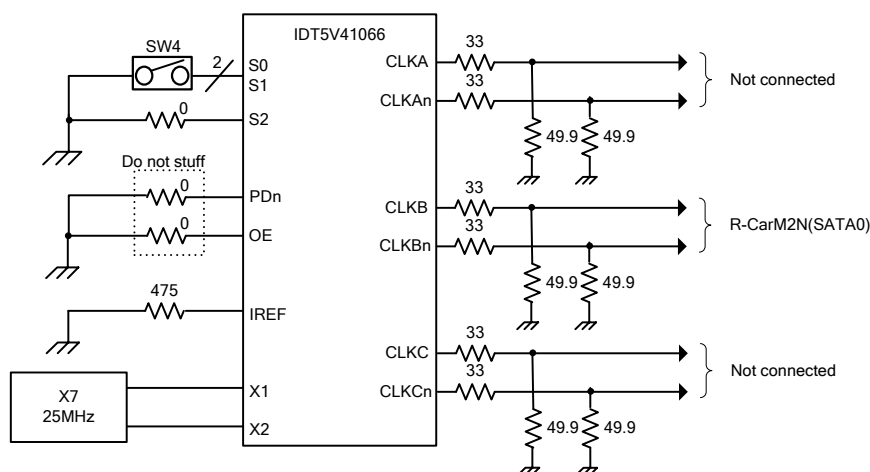


Figure 2.13.2 Block Diagram of Serial-ATA Clock Source

2.14. SD Card Host Interface 0 (SDHI0)

2.14.1. Specifications

The GOSE board incorporates an SD card slot (CN8) for the on-chip SD card host interface (SDHI0) of the R-CarM2N. For details on the SDHI0, see the R-Car Series, 2nd Generation User's Manual:Hardware.

On the GOSE board, the power (3.3 V) to be supplied to the VDD pin (pin 4 of CN8) of the SD card slot can be controlled by GP7_17. When GP7_17 is set to 1, power is supplied. When GP7_17 is set to 0, power is shut off.

On the GOSE board, the interface voltage (VCCQ_SD0) of the SD card slot can be selected by GP2_12. When GP2_12 is set to 1, 3.3 V is supplied as VCCQ_SD0. When GP2_12 is set to 0, 1.8 V is supplied as VCCQ_SD0.

Table 2.14.1 SD Card Host Interface (SDHI0) Specifications

| | |
|--|--|
| SD card host interface | R-CarM2N's on-chip SD card host interface channel 0 (SDHI0) |
| Voltage control for VDD (pin 4 of CN8) | VDD (pin 4 of CN8) = 3.3 V (GP7_17 = '1') VDD (pin 4 of CN8) = 0.0 V (GP7_17 = '0') |
| Interface voltage control | VCCQ_SD0 = 3.3 V (GP2_12 = '1') VCCQ_SD0 = 1.8 V (GP2_12 = '0') |
| SD card slot | DM1AA-SF-PEJ(82) by Hirose (CN8) |

2.14.2. Block Diagram

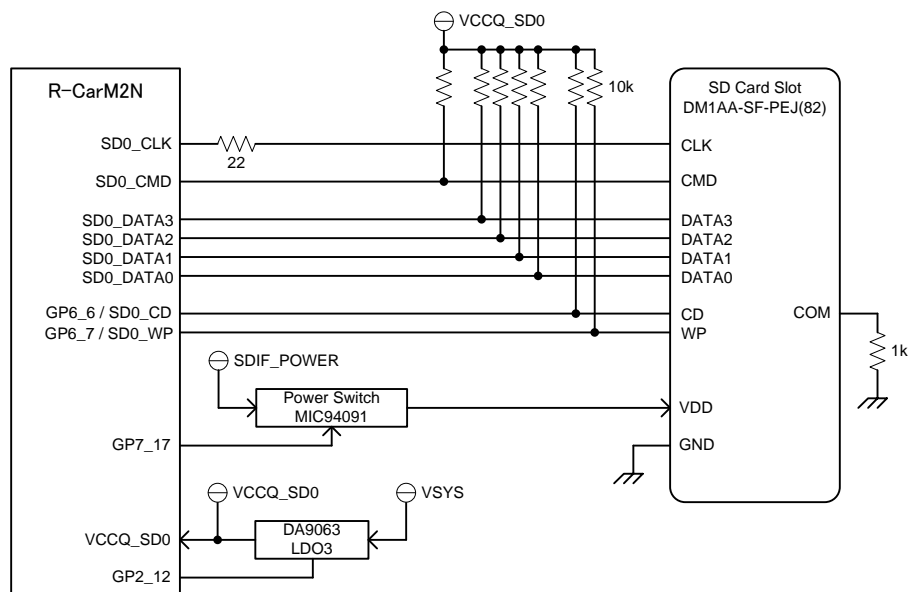


Figure 2.14.1 Block Diagram of SD Card Host Interface (SDHI0)

2.15. SD Card Host Interface 1 (SDHI1)

2.15.1. Specifications

The GOSE board incorporates an SD card slot (CN9) for the on-chip SD card host interface (SDHI1) of the R-CarM2N. For details on the SDHI1, see the R-Car Series, 2nd Generation User's Manual:Hardware.

On the GOSE board, the power (3.3 V) to be supplied to the VDD pin (pin 4 of CN9) of the SD card slot can be controlled by GP7_18. When GP7_18 is set to 1, the power is supplied. When GP7_18 is set to 0, the power is shut off.

On the GOSE board, the interface voltage (VCCQ_SD1) of the SD card slot can be selected by GP2_13. When GP2_13 is set to 1, 3.3 V is supplied as VCCQ_SD1. When GP2_13 is set to 0, 1.8 V is supplied as VCCQ_SD1.

When the SD card slot is used as the SDHI1 function set as follows.

(A1) Set JP3 to the pin 1 side. (A2) Set SW20 to the pin 1 side. (A3) Set SW21 to "OFF".

When the SD card slot is used as the DBG2 function, set as follows..

(B1) Set JP3 to the pin 3 side. (B2) Set SW20 to the pin 3 side. (B3) Set SW21 to "ON".

Table 2.15.1 SD Card Host Interface (SDHI1) Specifications

| | |
|--|--|
| SD card host interface | R-CarM2N's on-chip SD card host interface channel 1 (SDHI1) |
| Voltage control for VDD (pin 4 of CN9) | When JP3 is set to pin-1 side, VDD (pin 4 of CN9) = 3.3 V (GP7_18 = '1') VDD (pin 4 of CN9) = 0.0 V (GP7_18 = '0') |
| Interface voltage control | VCCQ_SD1 = 3.3 V (GP2_13 = '1') VCCQ_SD1 = 1.8 V (GP2_13 = '0') |
| SD card slot | DM1AA-SF-PEJ by Hirose (CN9) |

2.15.2. Block Diagram

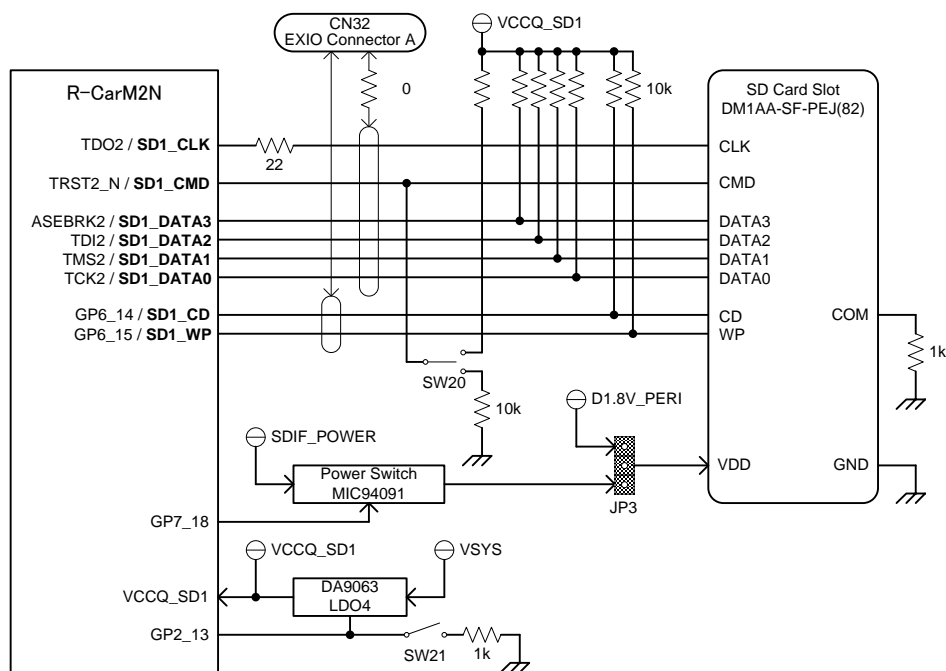


Figure 2.15.1 Block Diagram of SD Card Host Interface (SDHI1)

2.16. SD Card Host Interface 2 (SDHI2)

2.16.1. Specifications

The GOSE board incorporates a microSD card slot (CN12) for the on-chip SD card host interface (SDHI2) of the R-CarM2N. For details on the SDHI2, see the R-Car Series, 2nd Generation User's Manual:Hardware.

On the GOSE board, the power (3.3 V) to be supplied to the VDD pin (pin 4 of CN12) of the microSD card slot can be controlled by GP7_19. When GP7_19 is set to 1, power is supplied. When GP7_19 is set to 0, power is shut off.

On the GOSE board, the interface voltage (VCCQ_SD2) of the microSD card slot can be selected by GP2_26. When GP2_26 is set to 1, 3.3 V is supplied as VCCQ_SD2. When GP2_26 is set to 0, 1.8 V is supplied as VCCQ_SD2.

Table 2.16.1 SD Card Host Interface (SDHI2) Specifications

| | |
|---|--|
| SD card host interface | R-CarM2N's on-chip SD card host interface channel 2 (SDHI2) |
| Voltage control for VDD (pin 4 of CN12) | VDD (pin 4 of CN12) = 3.3 V (GP7_19 = '1') VDD (pin 4 of CN12) = 0.0 V (GP7_19 = '0') |
| Interface voltage control | VCCQ_SD2 = 3.3 V (GP2_26 = '1') VCCQ_SD2 = 1.8 V (GP2_26 = '0') |
| microSD card slot | DM3AT-SF-PEJM5 by Hirose (CN12) |

2.16.2. Block Diagram

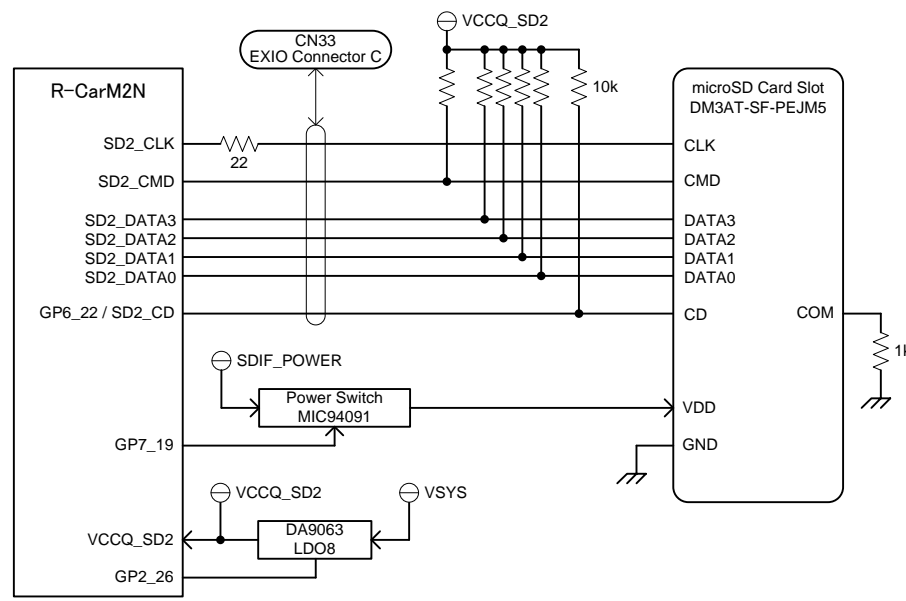


Figure 2.16.1 Block Diagram of SD Card Host Interface (SDHI2)

2.17. USB2.0 Interface

2.17.1. Specifications

The GOSE board has two USB2.0 ports that can be used as two USB2.0 host interface ports or one USB2.0 host interface port and one USB2.0 function interface port. The function interface is supported in channel 0.

The GOSE board incorporates a micro-AB connector as CN6 and a type A connector as CN5. For details, see the USB specifications in the R-Car Series, 2nd Generation User's Manual:Hardware and related datasheets.

Table 2.17.1 USB2.0 Specifications

| | |
|----------------------|--|
| USB controller | R-CarM2N's on-chip USB2.0 host and function controller |
| USB power supply | BD82065FVJ by ROHM Current limit: 2.4 [A] |
| USB host CN | R-CarM2N USB CH1 CN5: Type A connector XM7A-0442 by OMRON |
| USB host/function CN | R-CarM2N USB CH0 CN6: micro-AB connector ZX62D-AB-5P8 by Hirose |
| ESD protection diode | HZD6.2Z4 by Renesas |
| Common mode filter | DLM11SN900HY2 by Murata |
| Chip beads | BLM18PG330SN1D by Murata |

* The connector for channel 0 of the USB in the R-CarM2N is a micro connector shared by the USB host and function.

2.17.2. Block Diagram

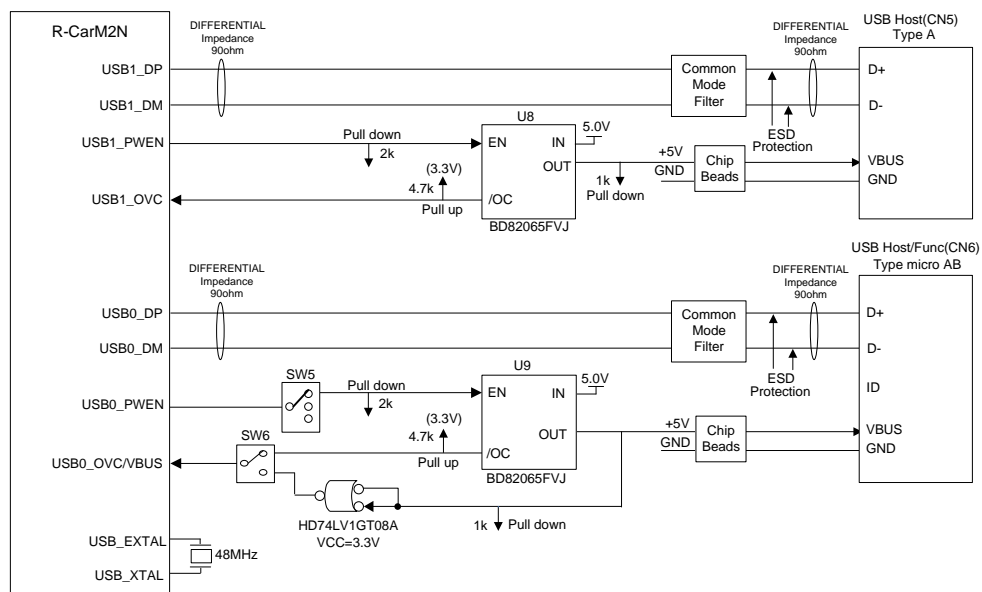


Figure 2.17.1 Block Diagram of USB2.0 Interface

2.18. Debug Serial Interfaces (SCIF0 and SCIF1)

2.18.1. Specifications

On the GOSE board, the SCIF0 (port D) and SCIF1 (port D) of the R-CarM2N are used as debug serial interfaces. The SCIF0 of the R-CarM2N is connected to the USB micro-AB connector (CN19) via the USB to UART bridge CP2102. Similarly, the SCIF1 is connected to CN20 via the CP2102 on the board. By connecting CN19 and CN20 to the host PC through USB cables, these interfaces can be used as 2-channel debug serial interfaces.

The SCIF_CLK pin of the R-CarM2N is connected to the crystal oscillator (X4) on the GOSE board, which supplies a clock frequency of 14.7456 MHz. When 14.7456 MHz is the frequency of the source clock, since the UART supports 300 bps to 1 Mbps due to the CP2102 device specifications, the maximum transfer rate becomes 921.6 kbps, which is obtained by dividing the source clock by 16. The SCIF0 and SCIF1 have the features shown below. For details, see the SCIF specifications in the R-Car Series, 2nd Generation User's Manual:Hardware.

- Asynchronous serial communications
- Full-duplex communication supported
- Selectable bit rates by using the R-CarM2N's on-chip baud-rate generator

The host PC connected to the GOSE board requires the CP2102 USB driver software. This driver software can be obtained from the following URL.

<http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx>

Table 2.18.1 Debug Serial Interface Specifications

| | |
|--------------------|--|
| Serial controller | R-CarM2N's on-chip SCIF0 (port D) and SCIF1 (port D) controllers |
| USB to UART bridge | CP2102 (1 Mbps max.) by Silicon Laboratories |
| Connector | CN19: SCIF0, ZX62D-AB-5P8 by Hirose CN20: SCIF1, ZX62D-AB-5P8 by Hirose |

2.18.2. Block Diagram

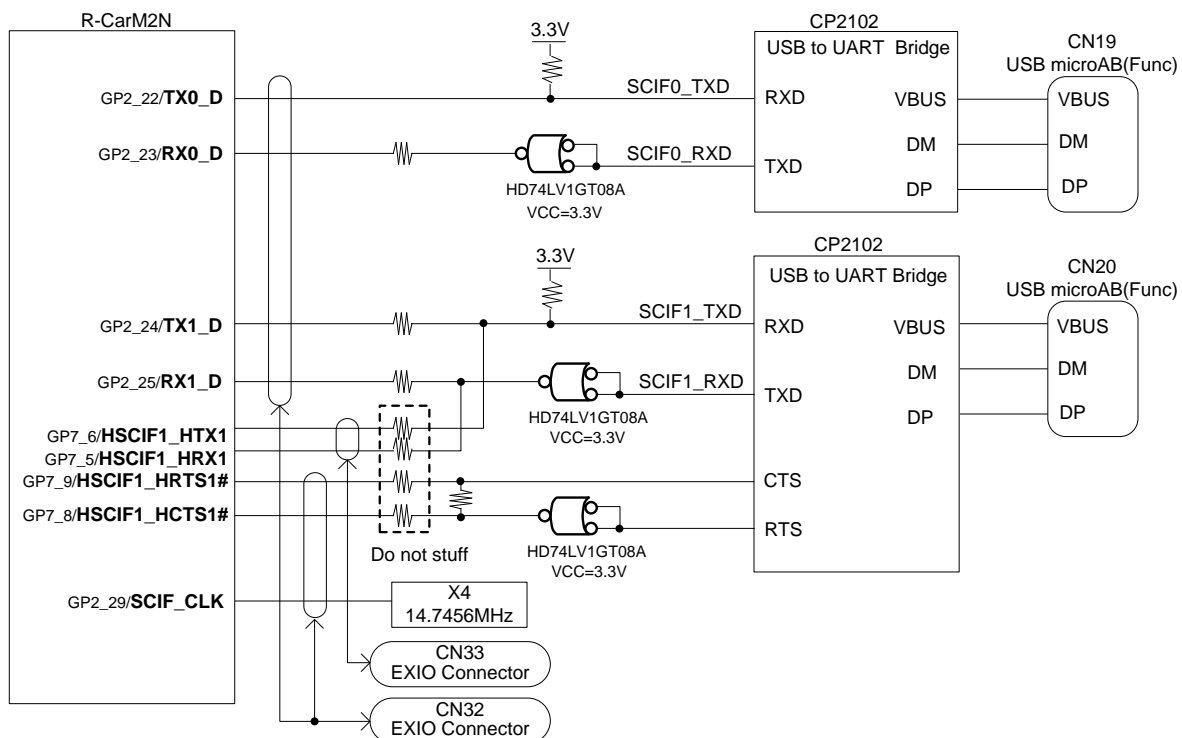


Figure 2.18.1 Block Diagram of Debug Serial Interface

2.19. External RTC (I²C Bus Interface)

2.19.1. Specifications

An external RTC (crystal resonator integrated type) such as RA-8581SA can be mounted on the GOSE board. **This is not mounted by default.** It connects to the R-CarM2N through the I²C interface (channel 1, port E). Since the GOSE board does not have a 3.3-V power supply for backup, the power to the external RTC is turned off when the ACC switch is off.

Due to the RA-8581SA specifications, the initial value for the interrupt (INT#) pin is undetermined after the power supply has settled at a desired voltage. This is because the initial values for the UIE, TIE, and AIE bits in the control register (Reg-F) of RA-8581SA are undetermined. When using interrupts from the external RTC, set the UIE, TIE, and AIE bits to 0 before de-masking the interrupts in the interrupt mask register of the R-CarM2N. See the RA-8581SA datasheet for details.

Table 2.19.1 External RTC (I²C) Specifications

| | |
|------------------------|---|
| External RTC interface | Via R-CarM2N's on-chip I ² C (channel 1, port E) |
| External RTC device | RA-8581SA by Seiko Epson (U34, Not mounted on the GOSE board) <ul style="list-style-type: none"> – Frequency adjusted 32.768-kHz crystal unit built in. – Time of day, calendar, alarm, timer, and other functions. – I²C slave address = 1010_001x, x = R/W# |

2.19.2. Block Diagram

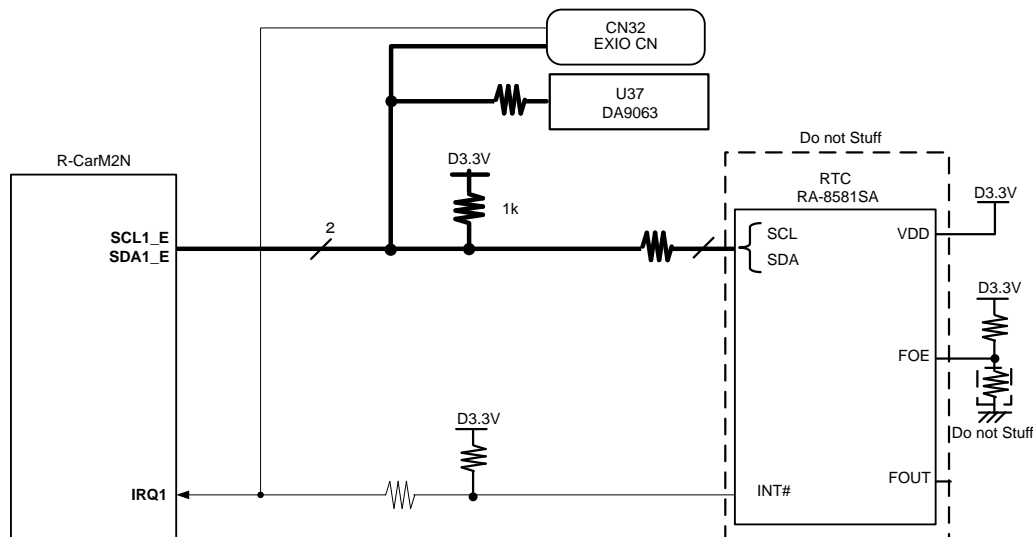


Figure 2.19.1 Block Diagram of External RTC Connection

2.20. Reset

2.20.1. Specifications

In the GOSE board specifications, the power-on reset signal is cleared by the reset IC MAX708SCSA, 200 ms after the 3.3-V power supply has settled. The power supplies for other voltage levels, 12.0 V, 5.0 V, 1.8 V, 1.35 V, and 1.0 V, are not monitored.

A power-on reset signal can be generated by pushing the push switch (SW7). The reset signal is level-shifted from 3.3 V to 1.8 V by the HD74ALVC1G07 and is input to the PRESET# pin of the R-CarM2N.

Table 2.20.1 RESET Specifications

| | |
|----------|---|
| | MAX708SCSA by Maxim Integrated |
| Reset IC | <ul style="list-style-type: none"> • Threshold voltage: 2.93 V • Reset delay time: 200 ms |

2.20.2. Block Diagram

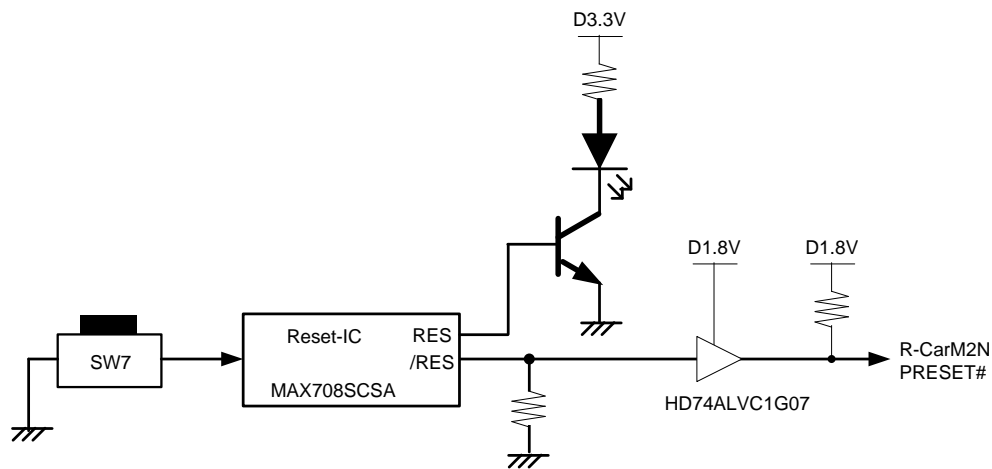


Figure 2.20.1 Block Diagram of Reset Circuit

2.21. I²C Interface

2.21.1. Specifications

The R-CarM2N incorporates seven I²C interface channels. Channels 5 and 6 are 1.8-V interfaces and channels 0 to 4 are 3.3-V interfaces.

The following devices are connected to each channel of the I²C interfaces on the GOSE board.

Table 2.21.1 I²C Interface Specifications

| | |
|--|--|
| I ² C controller | R-CarM2N's on-chip I ² C controller |
| I ² C devices through I ² C (ch6) | [1.8 V] CN33: EXIO connector C U37: DA9063 by Dialog Semiconductor U38: DA9210 by Dialog Semiconductor |
| I ² C devices through I ² C (ch5) | [1.8 V] CN29: Header pin (not mounted) |
| I ² C devices through I ² C (ch4 port C) | [3.3 V] CN28: Header pin (not mounted) CN30: EXIO connector E |
| I ² C devices through I ² C (ch3) | [3.3 V] CN34: EXIO connector D |
| I ² C devices through I ² C (ch2) | [3.3 V] U23: ADV7511WBSWZ by Analog Devices U29: ADV7612WBSWZ by Analog Devices U30: ADV7180WBCP32Z by Analog Devices U31: AK4643EN by AKM Semiconductor U50: R1EX24002ATAS0 by Renesas CN31: EXIO connector A CN34: EXIO connector D |
| I ² C devices through I ² C (ch1 port E) | [3.3 V] U34: RA-8581SA by Seiko Epson (not mounted) U37: DA9063 by Dialog Semiconductor CN32: EXIO connector B |
| I ² C devices through I ² C (ch0) | [3.3 V] CN31: EXIO connector A |

* I²C (ch3 and ch3 port B) signals are multiplexed with EtherMAC and VIN0 signal pins. They are connected to CN34, and when I²C (ch3 or ch3 port B) is used through CN34, the debug Ether and VIN0 interfaces on the GOSE board cannot be used.

* I²C (ch0) signals are multiplexed with LBSC signal pins. They are connected to CN31, and when I²C (ch0) is used through CN31, the A8 and A9 signals of the LBSC on the GOSE board cannot be used.

2.21.2. List of Slave Addresses

The table below lists the slave addresses of the I²C devices on the GOSE board.

Table 2.21.2 List of I²C Slave Addresses

| I ² C Ch | Ux CNx | Device | | SA7 | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | R/W# | Note |
|---------------------|--------|------------|---------------|-----|-----|-----|-----|-----|-----|-----|------|----------------------------|
| 6 | U37 | DA9063 | DCDC | - | - | - | - | - | - | - | - | - |
| | U38 | DA9210 | PMIC | - | - | - | - | - | - | - | - | - |
| | CN33 | EXIO CN C | Connector | - | - | - | - | - | - | - | - | - |
| 5 | CN29 | Header pin | Connector | - | - | - | - | - | - | - | - | Not mounted |
| 4 | CN28 | Header pin | Connector | - | - | - | - | - | - | - | - | Not mounted |
| | CN30 | EXIO CN E | Connector | - | - | - | - | - | - | - | - | - |
| 3 | CN34 | EXIO CN D | Connector | - | - | - | - | - | - | - | - | - |
| 2 | U23 | ADV7511 | HDMI Tx | 0 | 1 | 1 | 1 | 0 | 0 | 1 | X | Pin 22 (PD/AD) = GND |
| | U29 | ADV7612 | HDMI Rx | 1 | 0 | 0 | 1 | 1 | 0 | 0 | X | Pin 73 (ALSB) = GND |
| | U30 | ADV7180 | Video decoder | 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | Pin 26 (ALSB) = GND |
| | U31 | AK4643 | SSI CODEC | 0 | 0 | 1 | 0 | 0 | 1 | 0 | X | Pin 8 (CAD0) = GND |
| | U50 | R1EX24002 | I2C EEPROM | 1 | 0 | 1 | 0 | 0 | 0 | 0 | X | Pins 3 to 1 (A[2:0]) = GND |
| | CN31 | EXIO CN A | Connector | - | - | - | - | - | - | - | - | - |
| | CN34 | EXIO CN D | Connector | - | - | - | - | - | - | - | - | - |
| 1 | U34 | RA-8581SA | RTC | 1 | 0 | 1 | 0 | 0 | 0 | 1 | X | Not mounted |
| | U37 | DA9063 | PMIC | - | - | - | - | - | - | - | - | - |
| | CN32 | EXIO CN B | Connector | - | - | - | - | - | - | - | - | - |
| 0 | CN31 | EXIO CN A | Connector | - | - | - | - | - | - | - | - | - |

* I²C (ch3 and ch3 port B) signals are multiplexed with EtherMAC and VIN0 signal pins. They are connected to CN34, and when I²C (ch3 or ch3 port B) is used through CN34, the debug Ether and VIN0 interfaces on the GOSE board cannot be used.

* I²C (ch0) signals are multiplexed with LBSC signal pins. They are connected to CN31, and when I²C (ch0) is used through CN31, the A8 and A9 signals of the LBSC on the GOSE board cannot be used.

2.21.3. Block Diagram

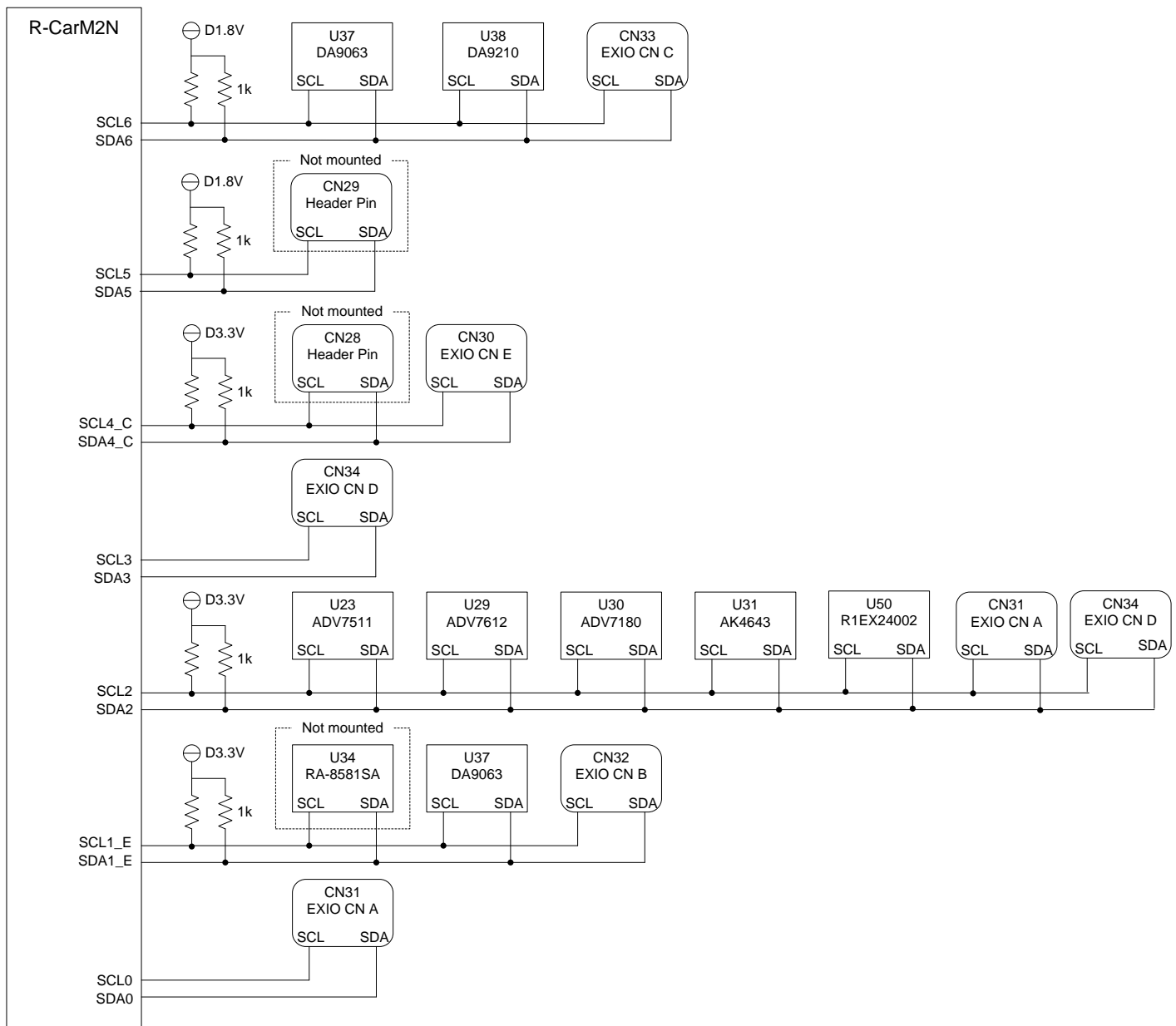


Figure 2.21.1 Block Diagram of I²C Interfaces

- * I²C (ch3 and ch3 port B) signals are multiplexed with EtherMAC and VIN0 signal pins. They are connected to CN34, and when I²C (ch3 or ch3 port B) is used through CN34, the debug Ether and VIN0 interfaces on the GOSE board cannot be used.
- * I²C (ch0) signals are multiplexed with LBSC signal pins. They are connected to CN31, and when I²C (ch0) is used through CN31, the A8 and A9 signals of the LBSC on the GOSE board cannot be used.

2.22. GPIO Interface (Software Switch, Tactile Switches, and General-Purpose LEDs)

2.22.1. Specifications

On the GOSE board, a 4-bit software switch (SW2), seven bits of tactile switches (SW30 to SW36), and three bits of LEDs (green) for debugging are incorporated. They are connected to the GPIO of the R-CarM2N as follows.

Table 2.22.1 List of Software Switch (General-Purpose Switch)

| GPIO | Software Switch |
|-------|----------------------|
| GP5_3 | Bit 3 (Pin 4 of SW2) |
| GP5_2 | Bit 2 (Pin 3 of SW2) |
| GP5_1 | Bit 1 (Pin 2 of SW2) |
| GP5_0 | Bit 0 (Pin 1 of SW2) |

Table 2.22.2 List of Tactile Switches (General-Purpose Switches)

| GPIO | Tact Switch |
|-------|--------------|
| GP7_6 | Bit 6 (SW36) |
| GP7_5 | Bit 5 (SW35) |
| GP7_4 | Bit 4 (SW34) |
| GP7_3 | Bit 3 (SW33) |
| GP7_2 | Bit 2 (SW32) |
| GP7_1 | Bit 1 (SW31) |
| GP7_0 | Bit 0 (SW30) |

Table 2.22.3 List of General-Purpose LEDs

| GPIO | LED |
|--------|----------------|
| GP2_21 | GP_LED2 (LED8) |
| GP2_20 | GP_LED1 (LED7) |
| GP2_19 | GP_LED0 (LED6) |

2.22.2. Block Diagram

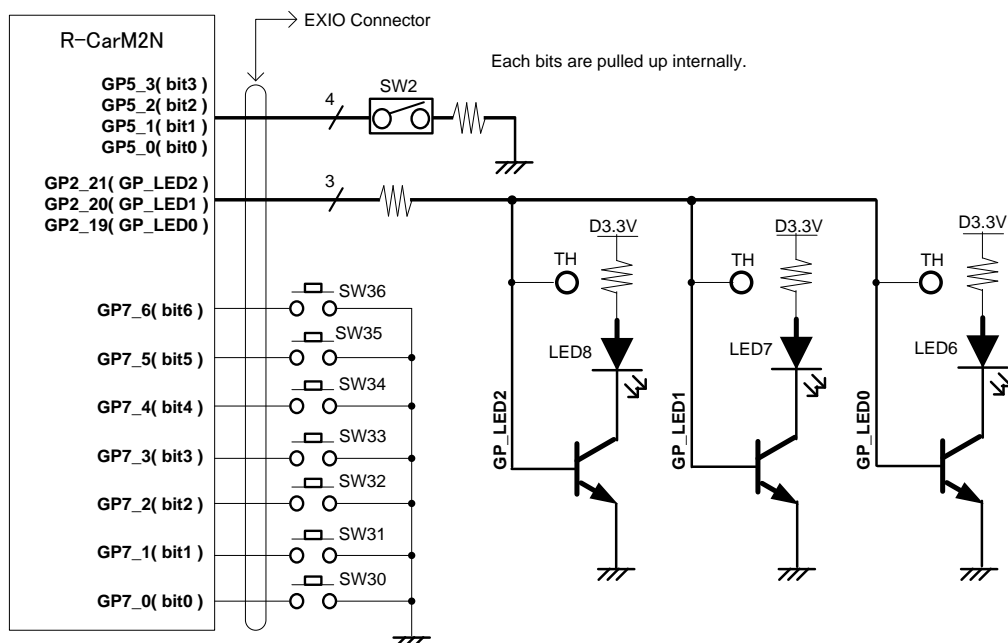


Figure 2.22.1 Block Diagram of GPIO Interface (Software Switch, Tactile Switches, and General-Purpose LEDs)

2.23. External Wait

2.23.1. Specifications

The R-CarM2N supports external wait requests from devices mapped to area 0 (CS0#), area 1 (CS1#), and expansion areas 0 to 5 (EX_CS0# to EX_CS5#). The R-CarM2N uses the LBSC to manage external waits.

The GOSE board does not incorporate a device to output WAIT or RDY requests. The only signal connected to the R-CarM2N is EXWAIT0#, which is output from the EX memory connector (CN7) and EXIO connector (CN31). The EXWAIT0# signal is pulled-up by a 10-kΩ resistor (R31) on the GOSE board, and a low level of this signal output to the R-CarM2N specifies a WAIT request.

Table 2.23.1 External Wait Control Interface Specifications

| Signal | Devices that Output the WAIT or RDY Request |
|----------|--|
| EX_WAIT0 | (1) WAIT# request from the EXIO connector A (CN31) (2) WAIT# request from the EX memory connector (CN7) |

2.23.2. Block Diagram

A block diagram of the external wait function is shown below.

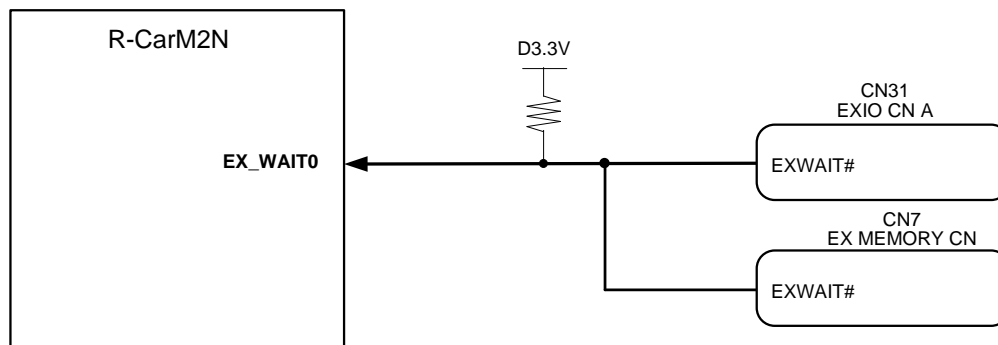


Figure 2.23.1 Block Diagram of External Wait Interface

2.24. External Interrupts

2.24.1. Specifications

The R-CarM2N has external interrupt input pins NMI, IRQ[9:0], INTC_IRQ[4:0]#, and INTC_EN[1:0]#.

The GOSE board uses IRQ0, IRQ1, and IRQ2 as external interrupt input pins, and GP3_29, GP4_2, and GP6_29 as GPIO interrupts. These pins should be used as active-low signals in programs.

For the interrupt functions of the R-CarM2N, see the R-Car Series, 2nd Generation User's Manual:Hardware.

The devices and connectors of the interrupt request sources on the GOSE board are shown below.

Table 2.24.1 External Interrupt Specifications

| Interrupt Pin | Devices that Output Interrupt Request | Connectors |
|---------------|---|--|
| IRQ0 | RMII PHY U21: KSZ8041RNLI by Micrel | CN32: EXIO connector B |
| IRQ1 | RTC U34: RA-8581SA by Seiko Epson (not mounted) | CN7: EX memory connector CN32: EXIO connector B |
| IRQ2 | PMIC U37: DA9063 by Dialog Semiconductor | CN32: EXIO connector B |
| GP3_29 | HDMI transmitter U23: ADV7511WBSWZ by Analog Devices | CN30: EXIO connector E |
| GP4_2 | HDMI receiver U29: ADV7612WBSWZ by Analog Devices | CN34: EXIO connector D |
| GP6_29 | MOSFET Driver U35: R2A11302FT by Renesas | CN32: EXIO connector B |

2.24.2. Block Diagram

A block diagram of external interrupts is shown below.

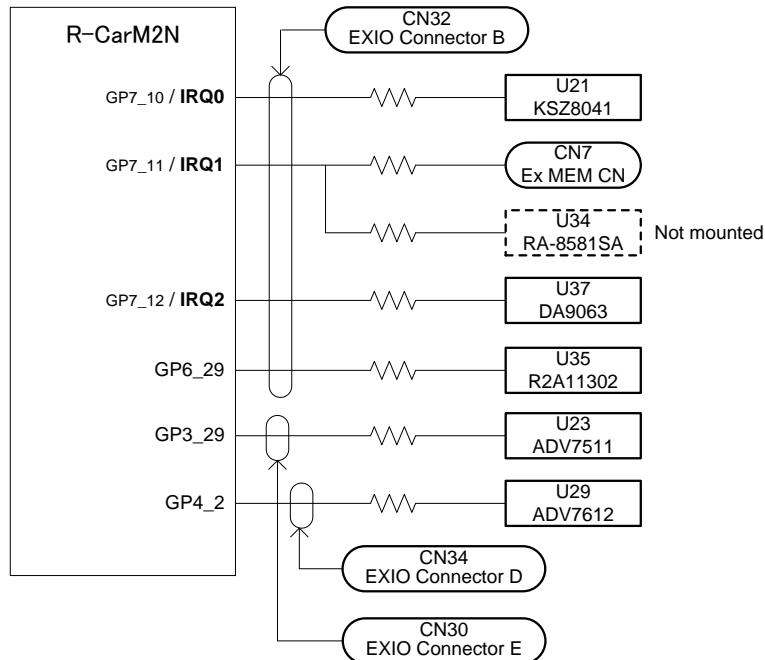


Figure 2.24.1 Block Diagram of External Interrupts

2.25. PWM

The R-CarM2N incorporates a seven-channel pulse width modulation timer (PWM). On the GOSE board, the use of other pin functions is given priority over the PWM functions in the case of pins that have multiplexed PWM functions. See the table below for details.

Table 2.25.1 Pin Functions Given Priority over PWM Functions

| PWM | Pin Functions Given Priority over PWM Functions |
|--------|---|
| PWM0 | SD1_CD to SDHI1 interface |
| PWM0_B | GPIO (GP5_30) |
| PWM1 | Mode pin 'MD8' |
| PWM1_B | SD1_WP to SDHI1 interface |
| PWM2 | LBSC 'BS#' |
| PWM2_B | LBSC address 'A0' |
| PWM3 | GPIO (GP1_24) |
| PWM4 | GPIO (GP3_26)/DU1_DOTCLKOUT1 |
| PWM4_B | Mode pin 'MD0' |
| PWM5 | GPIO (GP7_21) |
| PWM5_B | GPIO (GP7_20) |
| PWM6 | GPIO (GP7_22) |

2.26. TCLK for External Clock Input

The TCLK1 and TCLK2 pins can be selected as inputs for the external clock signal to the R-CarM2N's timer unit (TMU). On the GOSE board, the use of other pin functions is given priority over TCLK1 and TCLK2 in the case of pins that have multiplexed TCLK functions. See the table below for details.

Table 2.26.1 Pin Functions Given Priority over TCLK Functions

| TCLK pin | Pin Functions Given Priority over TCLK Functions |
|----------|--|
| TCLK1 | GPIO (GP7_0) |
| TCLK1_B | ETH_TX_EN for Ethernet communication |
| TCLK2 | GPIO (GP7_2) |

2.27. Clock

The GOSE board uses the crystal oscillators and resonators shown below.

2.27.1. Clocks Supplied to the R-CarM2N

Table 2.27.1 List of Clocks and Crystals for R-CarM2N

| No. | Xn | Frequency | Pin Name on R-CarM2N | Type | Remarks |
|-----|-----|-------------|----------------------|---------------------------------|---------|
| 1 | X1 | 48.0000 MHz | USB_XTAL, USB_EXTAL | Resonator | - |
| 2 | X2 | 74.25 MHz | DU1_DOTCLKIN | Oscillator, socket-mounted | - |
| 3 | X13 | 148.500 MHz | DU0_DOTCLKIN | Oscillator | - |
| 4 | X4 | 14.7456 MHz | SCIF_CLK | Oscillator | - |
| 5 | X5 | 20.0000 MHz | XTAL, EXTAL | Resonator (not mounted) | (*1) |
| 6 | X6 | 20.0000 MHz | EXTAL | Oscillator | (*2) |
| 7 | X15 | - | EXTAL | Socket (oscillator not mounted) | (*3) |

(*1) Not available for use at the same time as No.6 and No.7.

(*2) Not available for use at the same time as No.5 and No.7.

(*3) Not available for use at the same time as No.5 and No.6.

2.27.2. Clocks Supplied to Devices Other than R-CarM2N

Table 2.27.2 List of Clocks and Crystals Other than for R-CarM2N

| No. | Xn | Frequency | Device | Device Pin Name | Type |
|-----|-----|--------------|--|-------------------|------------|
| 1 | X7 | 25.0000 MHz | IDT5V41066 | X1, X2 | Resonator |
| 2 | X8 | 25.0000 MHz | KSZ8041RNLI | XI, XO | Resonator |
| 3 | X9 | 12.0000 MHz | ADV7511WBSWZ | CEC_CLK | Oscillator |
| 4 | X11 | 28.63636 MHz | U29: ADV7612WBSWZ U30: ADV7180WBCP32Z | XTALP XTAL | Oscillator |
| 5 | X12 | 11.2896 MHz | AK4643 | MCKI | Oscillator |
| 6 | X14 | 32.768 kHz | DA9063 | XTAL_IN, XTAL_OUT | Resonator |

2.28. Power Supply

2.28.1. Specifications

The GOSE board operates on a single 12.0-VDC power supply.

The power supplies used for the GOSE board are generated by the switching regulators and low-dropout regulators.

Take care to ensure the following two points:

- (1) The typical default value for overcurrent detection of the R2A11302FT is defined as 7 A in the specification. Therefore, configure your system so that the current generated by the R2A11302FT ICs and drawn by the VSYS (4.2 V) and D5.0V pins does not exceed 7 A.
- (2) Specified sequences should be used to turn on and off the power supply to the R-CarM2N. Be sure to control the ACC switch (SW25) to obey the power sequence on the GOSE board.

See the table below for regulators used to generate power supplies on the GOSE board, their input voltage (Vin) and output voltage (Vout), and whether the ACC switch can be used to enable or disable output of power supplies.

Table 2.28.1 List of GOSE Board Switching Controllers and Regulators

| Vin | Vout | Switching Controller and Regulator | Power MOSFET | ACC Switch Control |
|--|------------------------|---|------------------------------------|--------------------|
| Power Supply 12.0 VDC through CN24 or CN25 | D12.0V | - | - | Not supported |
| D12.0V | VSYS (D4.2V) | Renesas Electronics R2A11302FT (ch1 of U35) | Renesas Electronics HAT2210R (IC1) | Supported |
| | D5.0V | Renesas Electronics R2A11302FT (ch2 of U35) | Renesas Electronics HAT2210R (IC2) | Supported |
| | B1.35V/VTTO | Linear Technology LTC3634EFE#PBF (U48) | - | Supported |
| | D1.35V/VTT1 | Linear Technology LTC3634EFE#PBF (U49) | - | Supported |
| VSYS | D1.0V | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | D3.3V | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | D1.8V | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | D1.8V_PERI | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | VCCQ1.8V | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | VLDO3_SD0 (3.3/1.8 V) | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | VLDO4_SD1 (3.3/1.8 V) | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | VIO33 (3.3 V) | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | VLDO7_1.8V | Dialog Semiconductor DA9063 (U37) | - | Supported |
| | VLDO8_SD2 (3.3/1.8 V) | Dialog Semiconductor DA9063 (U37) | - | Supported |
| D5.0V | DVFS1.0V | Dialog Semiconductor DA9210 (U38) | - | Supported |
| D5.0V | LVDS_MON_POWER (3.3 V) | Analog Devices ADP3338AKCZ-3.3R7 (U28) | - | Supported |
| | SDIF_POWER (3.3 V) | Analog Devices ADP3339AKCZ-3.3R7 (U39) | - | Supported |

[Note]

As D12.0V is output to the following connectors, connecting or disconnecting an external board or a cable to these connectors must be performed while 12 V is not supplied to CN24 and CN25 (while the 100-VAC switch is off).

- Power supply connector for serial-ATA interface (CN2)
- Connector for INIC board (CN18)

However, since R449 (0 Ω) is not mounted at shipment, 12 V is not supplied to the connector for the INIC board (CN18).

- Connector for backlight (CN14)
- Power supply connector for EXIO board (CN26)

2.28.2. Block Diagram

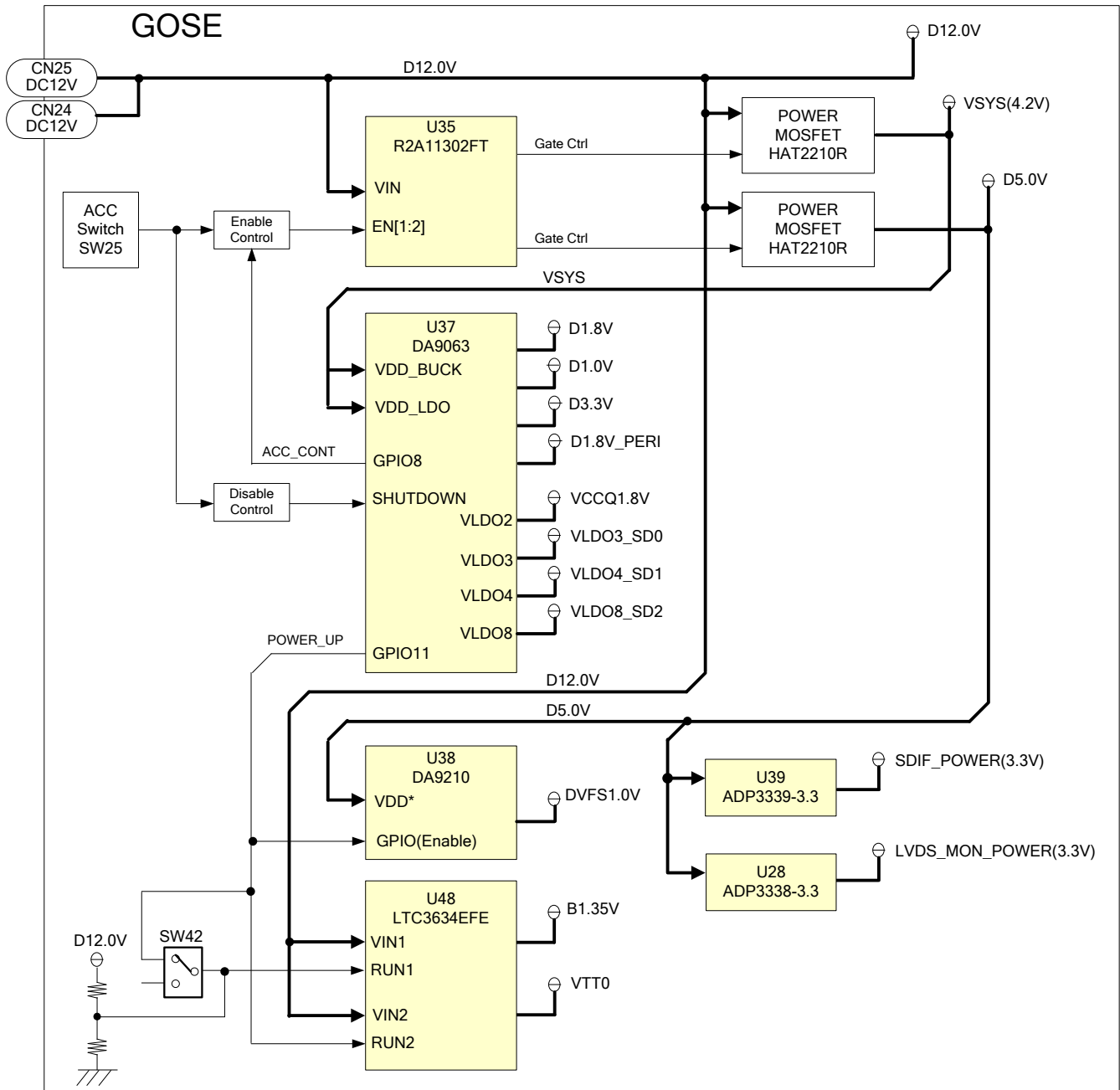
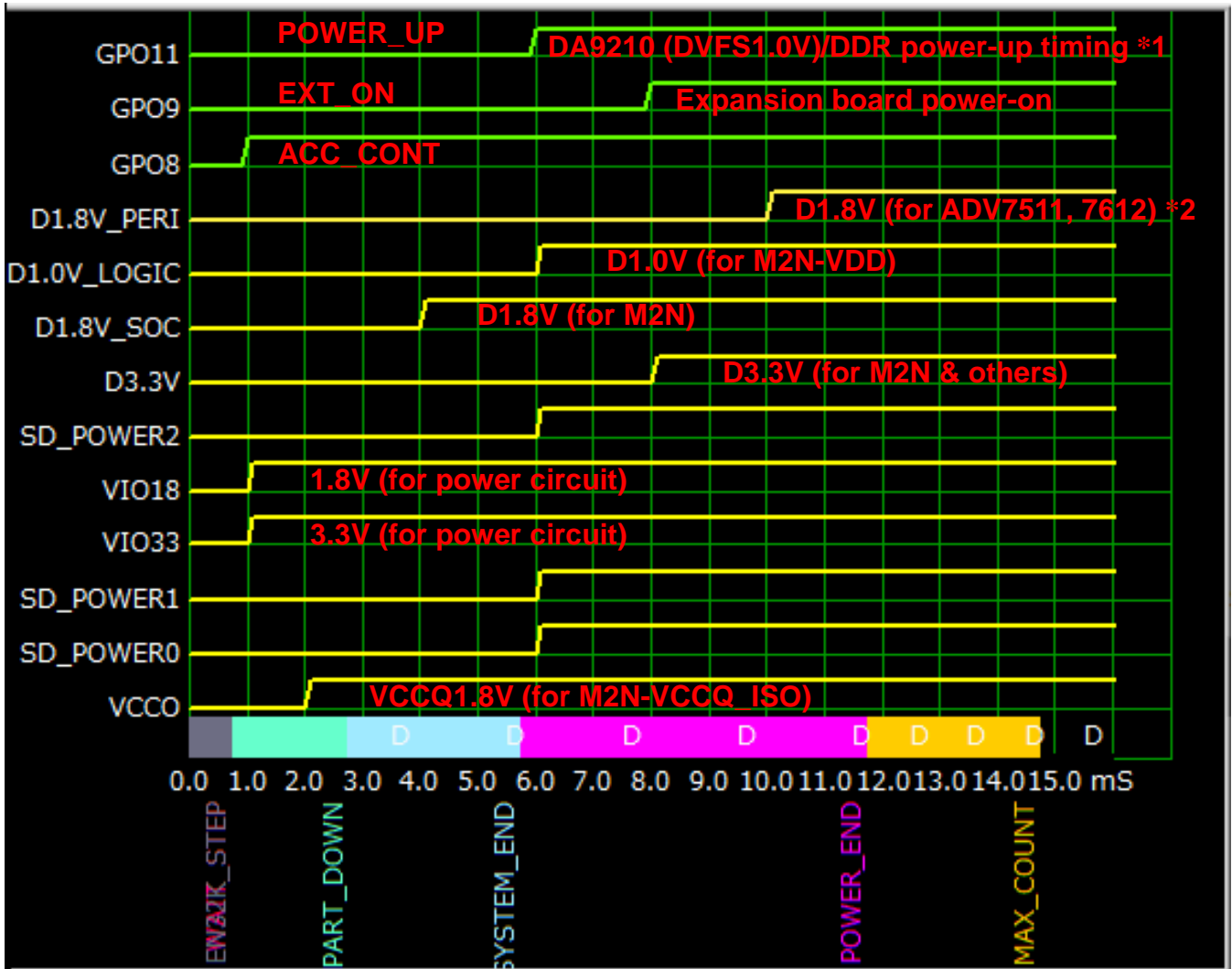


Figure 2.28.1 Block Diagram of Power Supply

2.28.3. Power-On Sequence

The diagram of the sequence for turning on the power (DA9063 OTP) to the GOSE board is shown below.



*1 The Co-PMIC (DA9210: DVFS1.0V) and DDR power (LTC3634: B1.35V, VTT0) are turned on with the power-up timing.

*2 For the ADV7612, 3.3 V should be turned on before 1.8 V.

*3 In the power-off sequence, turn off the power supplies in reverse order of the power-on sequence.

Figure 2.28.2 Power-On Sequence

2.29. EXIO Connectors (CN30, CN31, CN32, CN33, and CN34)

2.29.1. Specifications

On the GOSE board, the local bus and peripheral I/O signals of the R-CarM2N are connected to five connectors (CN30, CN31, CN32, CN33, and CN34). The arrangement of connectors and pins on the GOSE board is shown below.

Table 2.29.1 EXIO Connector Specifications

| | |
|-------------------------|--|
| EXIO connector A (CN31) | QSE-040-01-F-D-A (by Samtec), 80-pin, 0.8-mm pitch |
| EXIO connector B (CN32) | QSE-040-01-F-D-A (by Samtec), 80-pin, 0.8-mm pitch |
| EXIO connector C (CN33) | QSE-020-01-F-D-A (by Samtec), 40-pin, 0.8-mm pitch |
| EXIO connector D (CN34) | QSE-040-01-F-D-A (by Samtec), 80-pin, 0.8-mm pitch |
| EXIO connector E (CN30) | QSE-020-01-F-D-A (by Samtec), 40-pin, 0.8-mm pitch |

Table 2.29.2 List of EXIO Connector A (CN31) Pins

| Pin | Net Name | Pin | Net Name |
|-----|----------|-----|------------------|
| 1 | NC | 41 | swA20 |
| 2 | ExD0 | 42 | ExA4 |
| 3 | NC | 43 | swA21 |
| 4 | ExD1 | 44 | ExA5 |
| 5 | NC | 45 | swA22 |
| 6 | ExD2 | 46 | ExA6 |
| 7 | NC | 47 | swA23 |
| 8 | ExD3 | 48 | ExA7 |
| 9 | NC | 49 | swA24 |
| 10 | ExD4 | 50 | ExA8 |
| 11 | NC | 51 | swA25 |
| 12 | ExD5 | 52 | ExA9 |
| 13 | NC | 53 | MD10/BSn_3 |
| 14 | ExD6 | 54 | ExA10 |
| 15 | NC | 55 | CS0n_3 |
| 16 | ExD7 | 56 | ExA11 |
| 17 | NC | 57 | CS1n/A26_3 |
| 18 | ExD8 | 58 | ExA12 |
| 19 | NC | 59 | EXCS0n_3 |
| 20 | ExD9 | 60 | MD6/WE0n_3 |
| 21 | NC | 61 | EXCS1n_3 |
| 22 | ExD10 | 62 | MD4/WE1n_3 |
| 23 | NC | 63 | GP1_14 |
| 24 | ExD11 | 64 | MD12/RDn_3 |
| 25 | NC | 65 | EXWAIT0n_3 |
| 26 | ExD12 | 66 | GP1_20 |
| 27 | ExA13 | 67 | NC |
| 28 | ExD13 | 68 | MD9/GP1_15 |
| 29 | ExA14 | 69 | I2C2-SCL_3 |
| 30 | ExD14 | 70 | GP1_16 |
| 31 | ExA15 | 71 | I2C2-SDA_3 |
| 32 | ExD15 | 72 | MD8/GP1_17 |
| 33 | ExA16 | 73 | GND |
| 34 | ExA0 | 74 | MD7/GP1_25 |
| 35 | ExA17 | 75 | CLKOUT_3 |
| 36 | ExA1 | 76 | GP1_24 |
| 37 | ExA18 | 77 | GND |
| 38 | ExA2 | 78 | GND |
| 39 | ExA19 | 79 | PRESETOUTn_3 |
| 40 | ExA3 | 80 | POWERON_RESETn_3 |

Table 2.29.3 List of EXIO Connector B (CN32) Pins

| Pin | Net Name | Pin | Net Name |
|-----|-----------------|-----|-----------------|
| 1 | GND | 41 | GND |
| 2 | GND | 42 | GND |
| 3 | GP2_19 | 43 | GP7_9/MLB_DAT_3 |
| 4 | PWGD_A | 44 | SSI_SCK34_3 |
| 5 | GP2_20 | 45 | SSI_SCK0129_3 |
| 6 | ACC_nSHUTDOWN | 46 | SSI_WS34_3 |
| 7 | GP2_18 | 47 | SSI_WS0129_3 |
| 8 | GP7_20 | 48 | SSI_SDAT3_3 |
| 9 | GP2_17 | 49 | SSI_SDAT0_3 |
| 10 | GP7_21 | 50 | SSI_SDAT4_3 |
| 11 | SCIF0_TXD_3 | 51 | GND |
| 12 | GP7_22 | 52 | GND |
| 13 | GP2_21 | 53 | SSI_SDAT1_3 |
| 14 | MDT1/GP4_29 | 54 | SCIF0_RXD_3 |
| 15 | GP2_15 | 55 | SSI_SDAT2_3 |
| 16 | MDT0/GP4_30 | 56 | GP2_12 |
| 17 | GP2_16 | 57 | SSI_SDAT9_3 |
| 18 | GP4_31 | 58 | GP2_13 |
| 19 | GND | 59 | SCIF1_TXD_3 |
| 20 | GND | 60 | GP2_26 |
| 21 | EXIO_SD1_CLK_3 | 61 | GND |
| 22 | MSIOF0_SCK_3 | 62 | GND |
| 23 | EXIO_SD1_CMD_3 | 63 | SCIF1_RXD_3 |
| 24 | MSIOF0_SYNC_3 | 64 | I2C1-SCL_3 |
| 25 | EXIO_SD1_DAT3_3 | 65 | SCIF_CLK_3 |
| 26 | MSIOF0_TXD_3 | 66 | I2C1-SDA_3 |
| 27 | EXIO_SD1_DAT2_3 | 67 | GND |
| 28 | MSIOF0_RXD_3 | 68 | GND |
| 29 | EXIO_SD1_DAT1_3 | 69 | AUDIO_CLKA_3 |
| 30 | GP6_28 | 70 | GP7_17 |
| 31 | EXIO_SD1_DAT0_3 | 71 | GP2_30 |
| 32 | GP6_29 | 72 | GP7_18 |
| 33 | SD1_CD_3 | 73 | IRQ2n_3 |
| 34 | GP5_31 | 74 | GP7_19 |
| 35 | SD1_WP_3 | 75 | IRQ1n_3 |
| 36 | GP2_3 | 76 | MD5/GP2_31 |
| 37 | GP7_7/MLB_CK_3 | 77 | GND |
| 38 | GND | 78 | GND |
| 39 | GP7_8/MLB_SIG_3 | 79 | IRQ0n_3 |
| 40 | GP2_4 | 80 | PRESETOUTn_3 |

Table 2.29.4 List of EXIO Connector C (CN33) Pins

| Pin | Net Name | Pin | Net Name |
|-----|--------------|-----|-------------|
| 1 | GND | 21 | I2C6-SDA_18 |
| 2 | GND | 22 | 9063_GPIO7 |
| 3 | GP7_0 | 23 | GND |
| 4 | TRSTn_18 | 24 | GND |
| 5 | GP7_1 | 25 | SD2_CLK_3 |
| 6 | TDI_18 | 26 | SD0_CLK_3 |
| 7 | GP7_2 | 27 | SD2_CMD_3 |
| 8 | TMS_18 | 28 | SD0_CMD_3 |
| 9 | GP7_3 | 29 | SD2_DAT3_3 |
| 10 | TCK_18 | 30 | SD0_DAT3_3 |
| 11 | GP7_4 | 31 | SD2_DAT2_3 |
| 12 | TDO_18 | 32 | SD0_DAT2_3 |
| 13 | GP7_5 | 33 | SD2_DAT1_3 |
| 14 | ASEBRKn_18 | 34 | SD0_DAT1_3 |
| 15 | GP7_6 | 35 | SD2_DAT0_3 |
| 16 | PRESETINn_18 | 36 | SD0_DAT0_3 |
| 17 | NC | 37 | SD2_CD_3 |
| 18 | NMIn_18 | 38 | SD0_CD_3 |
| 19 | I2C6-SCL_18 | 39 | SD2_WP_3 |
| 20 | 9063_GPIO9 | 40 | SD0_WP_3 |

Table 2.29.5 List of EXIO Connector D (CN34) Pins

| Pin | Net Name | Pin | Net Name |
|-----|---------------|-----|------------------|
| 1 | GND | 41 | GND |
| 2 | GND | 42 | ETH_CRS_DV_3 |
| 3 | VIN0_CLK_3 | 43 | VIN1_CLK_3 |
| 4 | VIN0_G7 | 44 | ETH_RX_ER_3 |
| 5 | VIN0_CLKENB_3 | 45 | VIN1_DATA0_3 |
| 6 | VIN0_G6 | 46 | ETH_RXD0_3 |
| 7 | GP4_2 | 47 | VIN1_DATA1_3 |
| 8 | VIN0_G5 | 48 | GND |
| 9 | VIN0_HSYNC_3 | 49 | VIN1_DATA2_3 |
| 10 | VIN0_G4 | 50 | ETH_RXD1_3 |
| 11 | VIN0_VSYNC_3 | 51 | GND |
| 12 | VIN0_G3 | 52 | GND |
| 13 | GND | 53 | VIN1_DATA3_3 |
| 14 | VIN0_G2 | 54 | ETH_LINK_3 |
| 15 | VIN0_B7 | 55 | VIN1_DATA5_3 |
| 16 | VIN0_G1 | 56 | ETH_REF_CLK_3 |
| 17 | VIN0_B6 | 57 | VIN1_DATA6_3 |
| 18 | VIN0_G0 | 58 | ETH_TXD1_3 |
| 19 | VIN0_B5 | 59 | VIN1_DATA4_3 |
| 20 | GND | 60 | ETH_TX_EN_3 |
| 21 | VIN0_B4 | 61 | VIN1_DATA7_3 |
| 22 | VIN0_R7 | 62 | GND |
| 23 | VIN0_B3 | 63 | GND |
| 24 | VIN0_R6 | 64 | GP5_22 |
| 25 | VIN0_B2 | 65 | GP5_30 |
| 26 | VIN0_R5 | 66 | ETH_TXD0_3 |
| 27 | VIN0_B1 | 67 | GND |
| 28 | VIN0_R4 | 68 | ETH_MDC_3 |
| 29 | VIN0_B0 | 69 | I2C2-SCL_3 |
| 30 | VIN0_R3 | 70 | GND |
| 31 | GND | 71 | I2C2-SDA_3 |
| 32 | VIN0_R2 | 72 | GP5_25 |
| 33 | GP5_0 | 73 | GND |
| 34 | VIN0_R1 | 74 | GP5_26 |
| 35 | GP5_1 | 75 | PRESETOUTn_3 |
| 36 | VIN0_R0 | 76 | GP5_27 |
| 37 | GP5_2 | 77 | POWERON_RESETn_3 |
| 38 | GND | 78 | GP5_28 |
| 39 | GP5_3 | 79 | GND |
| 40 | ETH_MDIO_3 | 80 | GP5_29 |

Table 2.29.6 List of EXIO Connector E (CN30) Pins

| Pin | Net Name | Pin | Net Name |
|-----|-------------------------|-----|------------------|
| 1 | DU1_DR7 | 21 | DU1_DG3 |
| 2 | MD3/DU1_HSYNC_3 | 22 | DU1_DG0 |
| 3 | DU1_DR6 | 23 | DU1_DG2 |
| 4 | MD2/DU1_VSYNC_3 | 24 | DU1_DB1 |
| 5 | DU1_DR5 | 25 | DU1_DB7 |
| 6 | MD1/DU1_DISP_3 | 26 | DU1_DB0 |
| 7 | DU1_DR4 | 27 | DU1_DB6 |
| 8 | GP3_29/DU1_ODDF_3 | 28 | GND |
| 9 | DU1_DR3 | 29 | DU1_DB5 |
| 10 | MD0/DU1_CDE_3 | 30 | DU1_DOTCLKOUT0_3 |
| 11 | DU1_DR2 | 31 | DU1_DB4 |
| 12 | GP3_26/DU1_DOTCLKOUT1_3 | 32 | GND |
| 13 | DU1_DG7 | 33 | DU1_DB3 |
| 14 | NC (D3.3V) | 34 | DU1_DOTCLKIN_3 |
| 15 | DU1_DG6 | 35 | DU1_DB2 |
| 16 | DU1_DR1 | 36 | GND |
| 17 | DU1_DG5 | 37 | I2C4-SCL_3 |
| 18 | DU1_DR0 | 38 | PRESETOUTn_3 |
| 19 | DU1_DG4 | 39 | I2C4-SDA_3 |
| 20 | DU1_DG1 | 40 | D3.3V |

3. Outline Diagrams of GOSE Board

3.1. External Dimensions and Hole Locations of GOSE Board

The following shows the external dimensions and hole locations of the GOSE board. (Unit: mm)

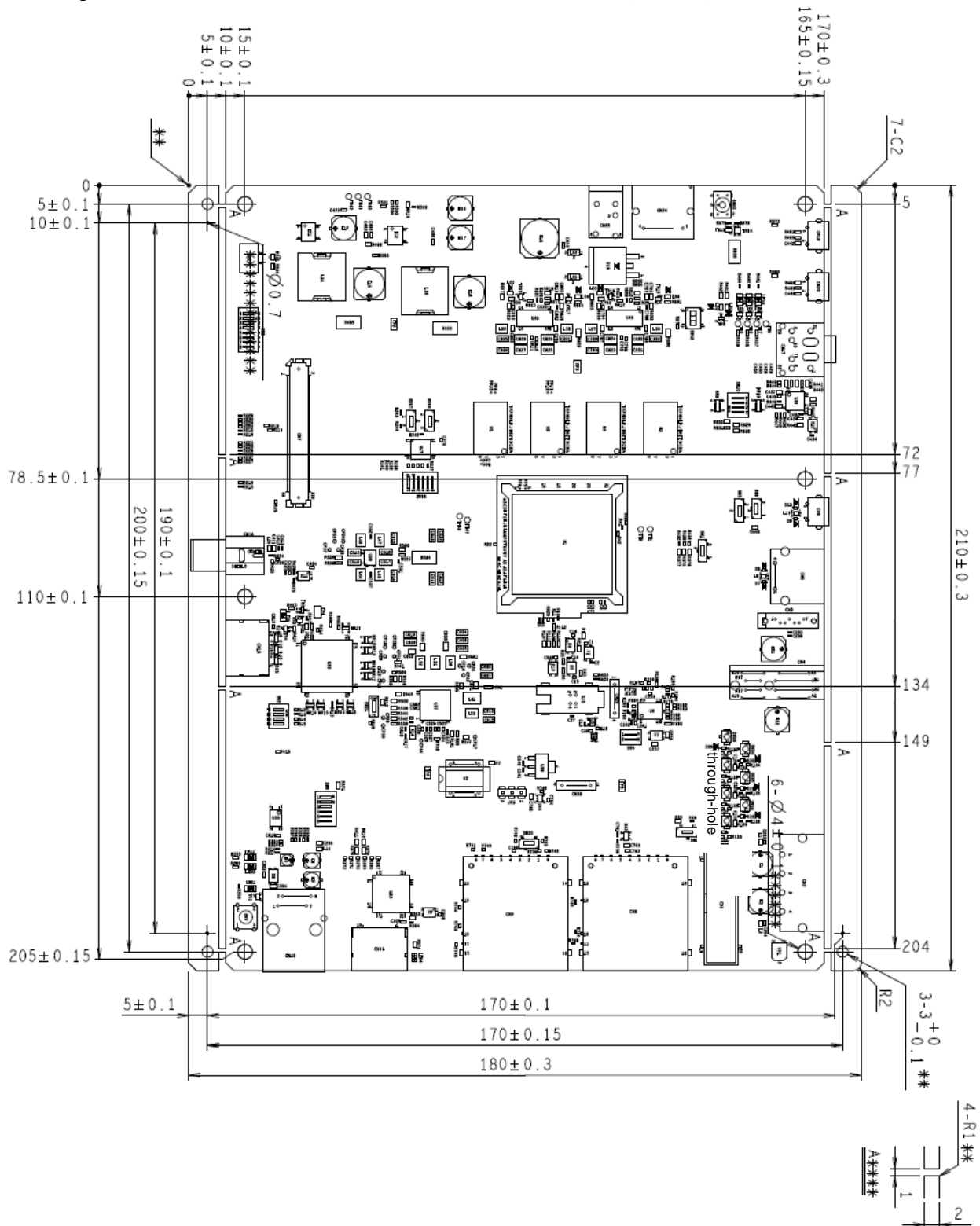


Figure 3.1.1 External Dimensions and Hole Locations of the GOSE Board

3.2. Connector Locations on GOSE Board (Component Surface)

The following shows the connector locations on the component surface. (Unit: mm)

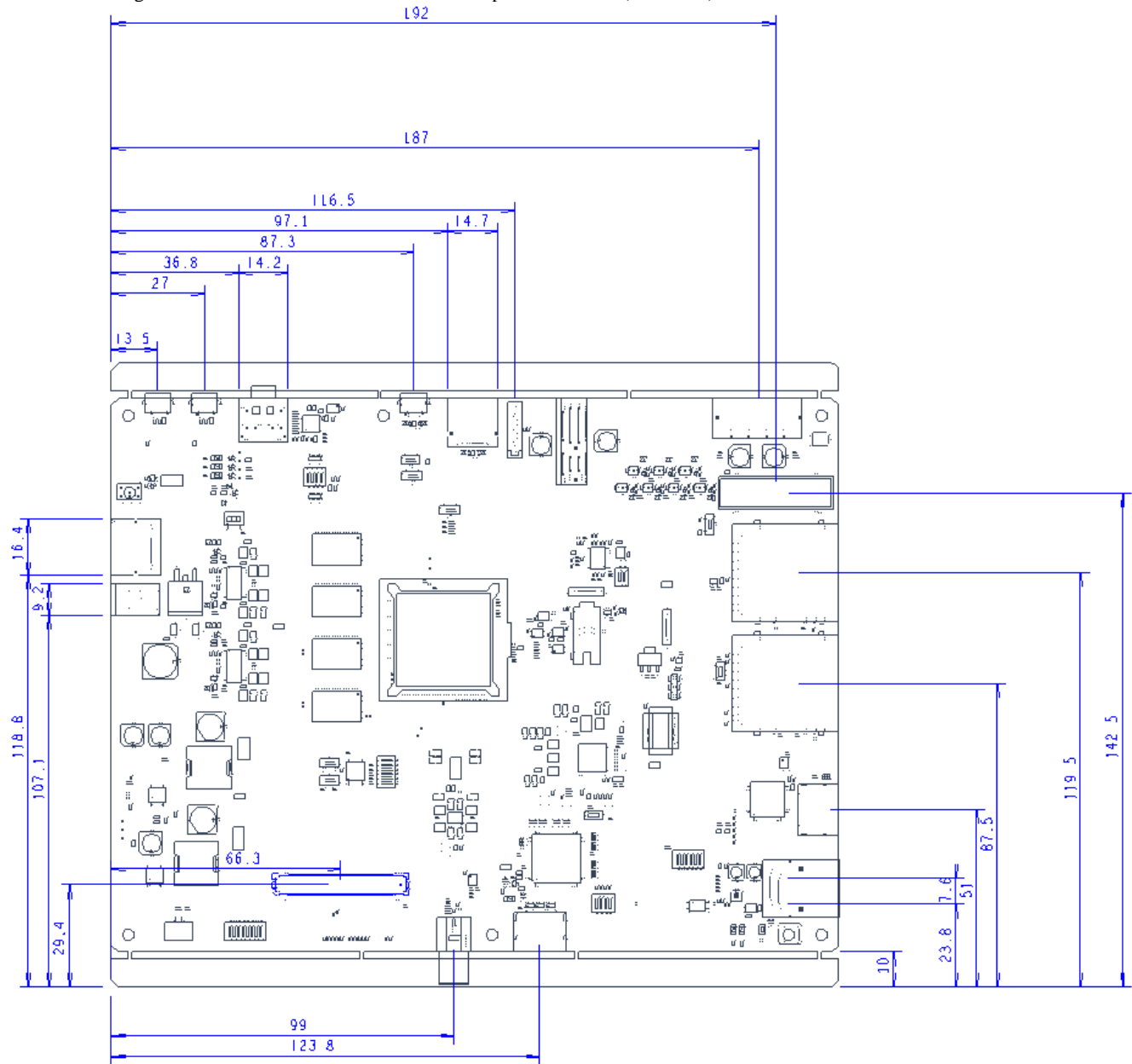
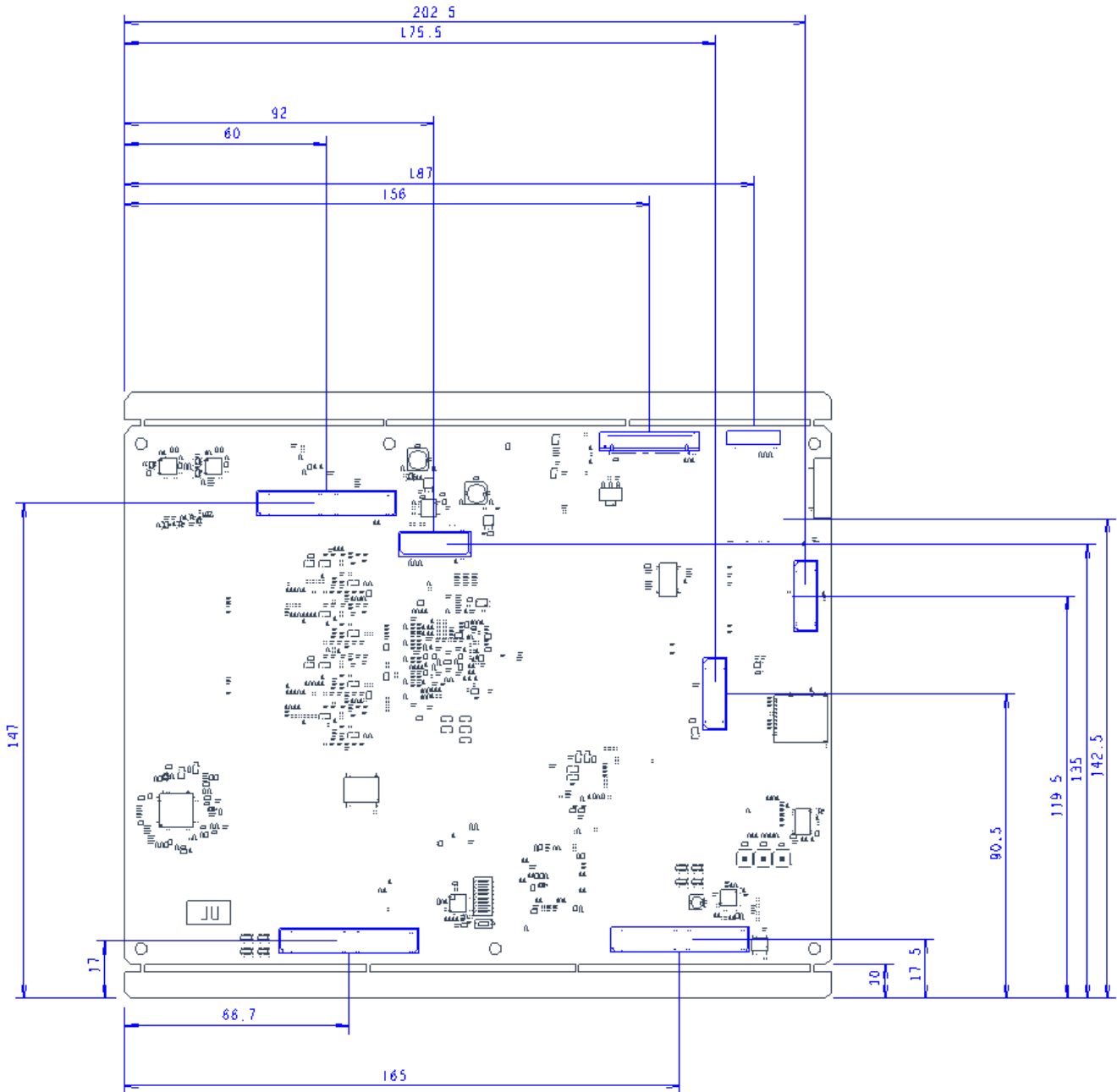


Figure 3.2.1 Connector Locations of the GOSE Board (Component Surface)

3.3. Connector Locations on GOSE Board (Solder Surface)

The following shows the connector locations on the solder surface. (Unit: mm)



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