P01: TITLE
P02: R-CarH3_SD/QSPI
P03: R-CarH3_DU/LBSC
P04: R-CarH3_USB/HDMI
P05: R-CarH3_NEW_POW1
P06: R-CarH3_NEW_POW2
P07: R-CarH3_LPDDR_POW
P08: HDMI_OUT/USB2.0/SD
P09: MMC0
P10: EtherAVB(GbPHY)
P11: Audio(AK4613VQ)
P12: DEBUG_SCIF/LED/TactSW
P13: R-CarH3_Mode_Setting
P14: R-CarH3_Module_I/F
P15: POWER PMIC

R-CarH3-SiP System Board "ULCB/H3 Sterter Kit"

RTP0RC7795SKB00010S

Rev.1.01

Title	R-CarH3-SiP System Board "ULCB/H3 Sterter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Sterter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 1 of 15	

Layout Note:
Following signals need Ground guard.

AUDIO_CLKA
AUDIO_CLKB
AUDIO_CLKC

HSCIF0_HSCK

AUDIO_CLKOUT
AUDIO_CLKOUT3

MSIOF0_SS2/AUDIO_CLKC

SCIF_CLK, SCIF_CLK until X1-pin3

SD0_CLK_V,SD0_CLK_SOC
SD3_CLK_V,SD3_CLK_SOC
MMC0_CLK_V,MMC0_CLK_SOC

AVB_TXCREFCLK
AVB_TXC_25
AVB_RXC_25

QSPI0_SPCLK_18, QSPI0_SPCLK
QSPI1_SPCLK_18, QSPI1_SPCLK

VTHSENSE0_18 until TH1
VTHREF0_18 until TH2

AUDIO_CLKA until X11-pin3
AUDIO_CLKB until U41-pin3
AUDIO_CLKOUT
EX_AUDIO_CLKA until X11-pin3
EX_AUDIO_CLKB until U41-pin3

Layout Note:
Following signals need Ground guard.

CLKOUT
QSPI0_SPCLK_18, QSPI0_SPCLK
QSPI1_SPCLK_18

AVB_TXCREFCLK (125MHz)

U1A

SRU(3.3V)

AUDIO_CLKA_A
GP5_12/HSCK0/AUDIO_CLKB_A
GP5_21/MSIOF0_SS2/AUDIO_CLKC_A
GP5_18/MSIOF0_SYNC/AUDIO_CLKOUT_A
GP5_19/MSIOF0_SS1/AUDIO_CLKOUT3_A

SSI(3.3V)

SSI_SCK0129
SSI_WS0129
SSI_SDATA0
SSI_SDATA1_A
GP6_08/SSI_SCK4
GP6_09/SSI_WS4
GP6_10/SSI_SDATA4

SCIF(3.3V)

GP6_23/AUDIO_CLKB_B/SCIF_CLK_A

SDHI0/DBG2(3.3V/1.8V)

SD0_WP
SD0_CD
SD0_DAT3/ASEBRK2
SD0_DAT2/TDI2
SD0_DAT1/TMS2
SD0_DAT0/TCK2
SD0_CMD/TRST2_N
SD0_CLK/TDO2

SDHI3(3.3V/1.8V)

GP4_16/SD3_DAT7/SD3_WP
GP4_15/SD3_DAT6/SD3_CD
GP4_12/SD3_DAT3
GP4_11/SD3_DAT2
GP4_10/SD3_DAT1
GP4_09/SD3_DAT0
GP4_08/SD3_CMD
GP4_07/SD3_CLK

MMC(3.3V/1.8V)_[SDHI1,2]

GP3_11/SD1_DAT3/SD2_DAT7
GP3_10/SD1_DAT2/SD2_DAT6
GP3_09/SD1_DAT1/SD2_DAT5
GP3_08/SD1_DAT0/SD2_DAT4
GP4_05/SD2_DAT3
GP4_04/SD2_DAT2
GP4_03/SD2_DAT1
GP4_02/SD2_DAT0
GP4_01/SD2_CMD
GP4_00/SD2_CLK
GP4_06/SD2_DS

GPIO

GPIO_Unused(1.8V/3.3V)

GP4_13/SD3_DAT4
GP4_14/SD3_DAT5
GP4_17/SD3_DS

GPIO_Unused(1.8V/3.3V)

GP3_06/SD1_CLK
GP3_07/SD1_CMD

GPIO_Unused(3.3V)

GP6_04/SSI_SDATA2_A
GP6_21/SSI_SDATA3_A

GPIO_PU

GP6_17/SSI_SCK78
GP6_18/SSI_WS78
GP6_19/SSI_SDATA7
GP6_20/SSI_SDATA8
GP5_13/HRX0
GP5_14/HTX0
GP5_15/HCTS0#
GP5_16/HRTS0#
GP5_24/MLB_SIG
GP5_25/MLB/IOEX_INTn

EtherAVB

AVB_RX_CTL_25 <10>
AVB_RXC_25 <10>
AVB_RD0_25 <10>
AVB_RD1_25 <10>
AVB_RD2_25 <10>
AVB_RD3_25 <10>
AVB_TX_CTL_25 <10>
AVB_TXC_25 <10>
AVB_TD0_25 <10>
AVB_TD1_25 <10>
AVB_TD2_25 <10>
AVB_TD3_25 <10>
AVB_TXCREFCLK
AVB_MDIO <10>
AVB_MDC <10>
GP2_10/AVB_MAGIC
AVB_PHY_INT <10>
AVB_LINK <10>
AVB_AVTP_MATCH/SCL5 <10,14>
AVB_AVTP_CAPTURE/SDA5 <10,14>

R724~R729:Close to U1(H3SiP)

QSPI(1.8V)

QSPI0_SPCLK
QSPI0_SSL
QSPI0_MOSI/IO0
QSPI0_MISO/IO1
QSPI0_IO2
QSPI0_IO3
QSPI1_SPCLK
QSPI1_SSL
QSPI1_MOSI/IO0
QSPI1_MISO/IO1
QSPI1_IO2
QSPI1_IO3
RPC_INT#
RPC_WP#
RPC_RESET#

T.SENSE(1.8V)

VTHSENSE0
VTHREF0

LVDS_bklight_Cnt

GP6_07/SSI_SDATA3
MSIOF1_TXD/LVDS_BLEN <13,14>

SoftSW

GP5_17/MSIOF0_SCK
GP5_20/MSIOF0_TXD
GP5_22/MSIOF0_RXD
GP5_23/MLB_CLK
GP5_23/MLB/SCL1 <14>

LED/TactSW

GP6_11/SSI_SCK5
GP6_12/SSI_WS5
GP6_13/SSI_SDATA5
GP_LED/TSW0 <12,13>
GP_LED/TSW1 <12,13>
GP_LED/TSW2 <12,13>

(3.3V) SDHI_PW

GP5_02/TX0
GP5_01/RX0
GP3_15/SD1_WP[wired or SDA0]
GP3_14/SD1_CD[wired or SCL0]
GP5_03/CTS0#
GP5_09/SCK2
SCIF0_TX/SD0_PWEN <8,14>
SCIF0_RX/SD0_VL <14,15>
SDA0/SD3_PWEN <14>
SCL0/SD3_VL <14,15>
SCIF0_CTSZ/SD1_VL <14>
SCIF2_SCK/SD2_VL <14>

BUS Switch

U89 SN74CB3Q3245RGYR

Select Function Table

OE	IN/OUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

QSPI_CPLDSW <13>

SPI FLASH (128Mbit/QSPI0)

QSPI0 Selector
1pin : SPI-FLASH
3pin : EX-SPI-Connector

U5 S25FS128SAGMFI10

EX-SPI Connector (QSPI0)

S25FS128SAGMFV10

S25FS 128 S AG M F V 10
##

- 10 = SOIC-8pin
- V = Automotive In-Cabin (-40C to +105C)
- F = Lead(Pb)-free
- M = SOIC
- AG = 133 MHz
- S = 0.65um MirrorBit Process Technology
- 128 = 128Mbit
- S25FS = Spansion Memory 1.8 Volt-Only

Audio Clock for 44.1kHz, 88.2kHz

#[AUDIO_CLKA]

X11 NZ2520SB_22.5792MHz/50ppm

[Design Note]
(fs=44.1kHz) * 256 = 11.2896MHz
(fs=88.2kHz) * 256 = 22.5792MHz
(fs=48.0kHz) * 256 = 12.2880MHz
(fs=96.0kHz) * 256 = 24.5760MHz

[Design Note]
There is a possibility of mount
to change the parts of the model number
X11 SG-210SCB 22.5792MHz L

SDHI0 (CLK,CMD,DAT[3:0])
(1) Matched trace length.

SDHI3 (CLK,CMD,DAT[3:0])
(1) Matched trace length.

MMC (CLK,CMD,DAT[7:0])
(1) Matched trace length.

Audio Clock for 48kHz, 96kHz, and for EtherAVB

#[AUDIO_CLKB]

U41 CS2000-CP

X12 NX2016SA_24.576MHz/20pF/15ppm

CL=20pF

[Design Note]
Ready for SPI access
by reworking.

[Design Note]
There is a possibility of mount
to change the parts of the model number
X12 CX2016DB24576D0PPSXX 24.576MHz

[CS2000-CP]
I2Cslave address: 1001_11px (p=AD0 pin,x=R/W#)
Read:0x9F, Write: 0x9E (AD0=1) for ULCB
Read:0x9D, Write: 0x9C (AD0=0) for EtherAVB PHY board.

[Design Note]
Selects PLL Lock/Unlock Indication.
Set AuxOutSrc[1:0]=11 and set AuxLockCfg=1

[Design Note]
There is a possibility of mount
to change the parts of the model number
X10 SG-8003CG 125.000000MHz SCB

[Design Note]
Hyper Flash of switching QSPI_CPLDSW

[Design Note]
There is a possibility of mount
to change the parts of the model number
X1 SG-210SCB 14.745600 MHz L

SERIES_TERM

Do not stuff

Note: "SD0_WP"and "SD0_CD" signal is fixed at 3.3V.

Note: "SD3_WP"and "SD3_CD" signal changes to 1.8V and 3.3V by the voltage supplied to the VDDQVA_SD3.

Note: "SD3_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VDDQVA_SD3.

Note: "SD1_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VDDQVA_SD1.
Unused
Unused

Matched trace length.
Trace like as differential pair.

After tying the GND side of both Cx and Cx, tie to the internal GND plane.

[Design Note]
Hyper Flash1 internal folded.
Hyper Flash0 external flash switching.

SMT PinHeader

H3SiP_BGA_r0096_005

R-CarH3SiP

R-CarH3 SDHI/QSPI/QSPI_FLASH

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 2 of 15	

[Design Note]
There is a possibility of mount
to change the parts of the model number

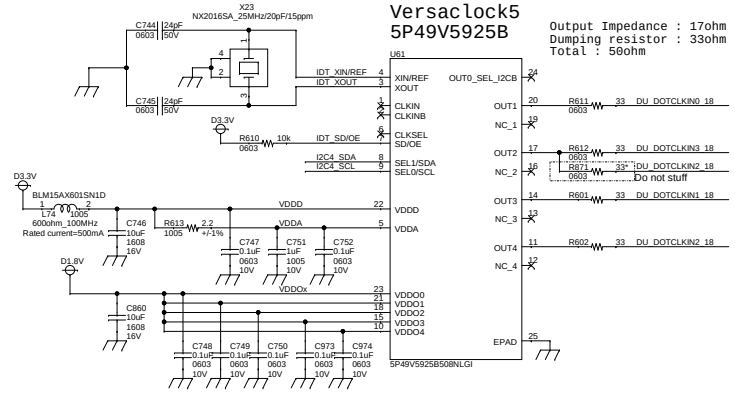
X23 FA-128 25.000000 MHz 20.0 +10.0-10.0

CL = 20pF(typ.)

I2Cslave address: 1101_010X
Read:H'D5 Write: H'D4

Versaclock5
5P49V5925B

Output Impedance : 17ohm
Dumping resistor : 33ohm
Total : 50ohm



Note.
1. Set OEn bit to output clock.
2. I2C is 3.3V signal.
3. C752(0.10uF) is for pin 5

Versaclock5 have Internal Pull-down Resistor(100k-300k)
CLKIN
CLKINB
SEL1/SDA
SEL0/SCL
OUT0_SEL_I2CB --> 0 = Use I2C (Default)
CLKSEL --> 0 = XIN/REF, XOUT (Default)
1 = CLKIN, CLKINB
SD/OE --> = OE and active low

Layout Note:
Following signals need Ground guard.

DU_DOTCLKIN0_18
DU_DOTCLKIN0_18 until U61-pin20
DU_DOTCLKIN1_18
DU_DOTCLKIN1_18 until U61-pin14
DU_DOTCLKIN2_18
DU_DOTCLKIN2_18 until U61-pin11
DU_DOTCLKIN3_18
DU_DOTCLKIN3_18 until U61-pin17
EXTAL_18 until X4-pin3

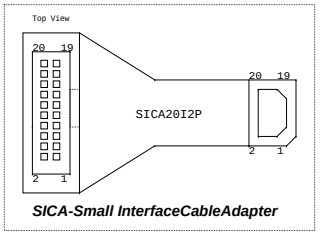
EXT_LPO

EXTALR_SOC, EXTALR_SOC until X5-pin3,

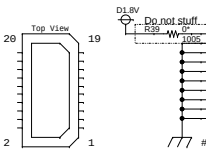
CLKOUT_SOC,CLKOUT

TCK_18

WE0n [CAN_CLK(40MHz)]



SICA-Small InterfaceCableAdapter



Be carefull !!
See Pin Assignment.

U1B

DU_CLK(1.8V)

DU_DOTCLKIN0_18 AP7 → DU_DOTCLKIN0
DU_DOTCLKIN1_18 AP8 → DU_DOTCLKIN1
DU_DOTCLKIN2_18 AR7 → DU_DOTCLKIN2
DU_DOTCLKIN3_18 AR8 → DU_DOTCLKIN3

CPG(1.8V)

AC39 XTAL
AC38 EXTAL
AD38 FSCLKST
AD39 EXTALR

X4 1.8V NZ2520SB_16.6666MHz/50ppm
R24 0 0603 EXTAL_18
C21 0.1uF 0603 10V

[Design Note]
There is a possibility of mount
to change the parts of the model number
X4 SG-210SEB 16.666600 MHz L

<14> FSCLKST
<14> EXT_LPO
R26 0 0603 EXTALR_SOC

X5 1.8V NZ2520SB_32.768kHz/50ppm
C22 0.1uF 0603 10V
R27 0 0603

[Design Note]
There is a possibility of mount
to change the parts of the model number
X5 KC2520M32K7680CM3E00

RESET

<2,9,13,14,15> PRESETn_18 → AR28 PRESET# 1.8V
<10,11,13,14> PRESETOUTn → C1 PRESETOUT# 3.3V
R33 100k 0603

DBG(1.8V)

TRST# AR26
TDI AR29
TMS AR30
TCK AT27
TDO AT28
ASEBRK AT30

<14> TRSTn_18
<14> TDI_18
<14> TMS_18
<14> TCK_18
<14> TDO_18
R35 4.7k 0603
R36 4.7k 0603
R37 4.7k 0603
R34 4.7k* 0603 Do not stuff
R38 1k 0603

20pin ARM_EML
CN3 #[ARM_20pin] SICA2P20S05
R40 0 1005
R42 0 0603
R44 0 0603
R46 0 0603
R47 0 0603
R48 0 0603 PRESETn_18
R49 0* 0603 ASEBRK_18 Do not stuff
R39 0* 1005 Do not stuff
R50 10k 0603
C25 0.1uF 0603 10V

R42,R44,R46,R47,R49:Close to CN1
R48:Close to U1(H3SiP)

H3SiP_BGA_r0096_005

R-CarH3SiP

LBSC_D(3.3V)

D15 R1 ExD15 DU_DR7 GP0_15 VI4_DATA7_A
D14 R2 ExD14 DU_DR6 GP0_14 VI4_DATA6_A
D13/MD10 T1 ExD13 DU_DR5 GP0_13 VI4_DATA5_A
D12/MD9 T2 ExD12 DU_DR4 GP0_12 VI4_DATA4_A
D11/MD8 U1 ExD11 DU_DR3 GP0_11 VI4_DATA3_A
D10/MD7 U2 ExD10 DU_DR2 GP0_10 VI4_DATA2_A
D9/MD6 V1 ExD9 DU_DR1 GP0_09 VI4_DATA1_A
D8/MD12 V2 ExD8 DU_DR0 GP0_08 VI4_DATA0_A
D7/MD5 W1 ExD7 GP0_07 VI4_DATA23 VI5_DATA7
D6/MD4 W2 ExD6 GP0_06 VI4_DATA22 VI5_DATA6
D5/MD3 Y1 ExD5 GP0_05 VI4_DATA21 VI5_DATA5
D4/MD11 Y2 ExD4 GP0_04 VI4_DATA20 VI5_DATA4
D3/MD2 AA1 ExD3 GP0_03 VI4_DATA19 VI5_DATA3
D2/MD1 AA2 ExD2 GP0_02 VI4_DATA18 VI5_DATA2
D1/MD0 AB2 ExD1 GP0_01 VI4_DATA17 VI5_DATA1
D0 AB1 ExD0 GP0_00 VI4_DATA16 VI5_DATA0

ExD[0..15] <13,14>

LBSC_A/DU(3.3V)

IRQ3/A25/DU_DOTCLKOUT1 A4 ExA25/PWM4 <13,14>
IRQ4/A24/DU_EXHSYNC/DU_HSYNC A3 ExA24/DU_EXHSYNC_DU_HSYNC <13,14>
IRQ5/A23/DU_EXVSYNC/DU_VSYNC B3 ExA23/DU_EXVSYNC_DU_VSYNC <13,14>
PWM0/A22 B6 ExA22/PWM0 <10,13,14>
PWM1_A/A21[wired or SCL3] A5 ExA21/PWM1 <13>
PWM2_A/A20[wired or SDA3] A6 ExA20/PWM2 <13,14>
ExA[0..19] <10,13,14>

A19/DU_DG3/MD13 E1 ExA19 DU_DG3 GP1_19 VI4_CLKENB
A18/DU_DG2/MD14 E2 ExA18 DU_DG2 GP1_18 VI4_HSYNC#
A17/DU_DG1/MD15 E3 ExA17 DU_DG1 GP1_17 VI4_VSYNC#
A16/DU_DG0/MD16 F3 ExA16 DU_DG0 GP1_16 VI4_FIELD
A15/DU_DG7/MD17 G1 ExA15 DU_DG7 GP1_15 VI5_DATA11
A14/DU_DG6/MD18 G2 ExA14 DU_DG6 GP1_14 VI5_DATA10
A13/DU_DG5/MD19 H1 ExA13 DU_DG5 GP1_13 VI5_DATA9
A12/DU_DG4/MD21 H2 ExA12 DU_DG4 GP1_12 VI5_DATA8
J1 ExA11 GP1_11 VI5_FIELD
A10/MD20 J2 ExA10 GP1_10 VI5_HSYNC#
A9 K1 ExA9 GP1_09 VI5_VSYNC#
A8 K2 ExA8 GP1_08
A7/DU_DB7/MD22 L1 ExA7 DU_DB7 GP1_07 VIx_DATA15
A6/DU_DB6/MD23 L2 ExA6 DU_DB6 GP1_06 VIx_DATA14
A5/DU_DB5/MD24 M1 ExA5 DU_DB5 GP1_05 VIx_DATA13
A4/DU_DB4/MD25 M2 ExA4 DU_DB4 GP1_04 VIx_DATA12
A3/DU_DB3/MD26 N1 ExA3 DU_DB3 GP1_03 VI4_DATA11
A2/DU_DB2 N2 ExA2 DU_DB1 GP1_02 VI4_DATA10
A1/DU_DB1/MD27 P1 ExA1 DU_DB1 GP1_01 VI4_DATA9
A0/DU_DB0/MD28 P2 ExA0 DU_DB0 GP1_00 VI4_DATA8

LBSC/DU(3.3V)

SERIES_TERM

CLKOUT F1 CLKOUT_SOC 22 R23 0603 CLKOUT <14>
CS1#/A26 F4 CS1n/A26 <14>
CS0# C2 CS0n <13,14> VI5_CLK
WE1# D2 R856 0 0603 WE1n/GP1_26/CAN1_RX <13,14> VI5_CLKENB
WE0# B1 R857 0 0603 WE0n/GP1_25/CAN_CLK <14>
BS#/MD0 C4 R858 0 0603 MD0/BSn/GP1_22/CAN1_TX <13,14>
RD#/MD1 A2 R859 0 0603 MD1/RDn/GP1_23/CAN0_TX <13,14>
GP1_24/RD_WR# D3 R860 0 0603 RD/WR#/GP1_24/CAN0_RX <13,14>
TP4 HK-2-G

[Design Note]
CAN Signal (CAN_CLK , CAN0 TX/RX , CAN1 TX/RX)
A 0 Ohm in the line as short as possible to the SIP
(overall length including SIP layout should be <= 30mm).
Same length from H3 device to each of this 0 Ohm.
If possible a GND testpoint near by the 0 Ohm resistors.

D3.3V R25 10k 0603
EX_WAIT0_A/DU_DOTCLKOUT0 D1 EX_WAIT0n/DU_DOTCLKOUT0 V14_CLK <14>
GP2_02/IRQ2/DU_EXODDF/DU_ODDF/DISP/CDE B4 PWM3/IRQ2n/DU_DISP <14>
EX_WAIT0 : ExMEM
IRQ2# : ExMEM

INTC

D1.8V R28 10k 0603
IRQ0# : PMIC
1.8V NMI AT29 NMIn_18 <14>
3.3V IRQ0 B5 GP2_00/IRQ0n <14,15>
3.3V IRQ1 A5 DU_DISP/IRQ1n <14>

I2C(3.3V)

D3.3V R29 1k 0603 R30 1k 0603 R31 1k 0603 R32 1k 0603
GP5_04/RTS0#/TANS/SCL2_A G39 SCIF0_RTSZ/I2C2_SCL <2,11,14>
GP5_00/SCK0/SDA2_A K39 SCIF0_SCK/I2C2_SDA <2,11,14>
SCL4 AD1 I2C4_SCL <12,14>
SDA4 AD2 I2C4_SDA <12,14>

IIC_DVFS(3.3V)

D3.3V R706 1k 0603 D3.3V R707 1k 0603
C817 0.1uF 0603 10V
U68 TXS0102DCUT
V3P3 C818 0.1uF 0603 10V
IIC_DVFS is pulled-up to V3P3 at page of PMIC.
SCL_DVFS AC1 SCL_DVFS
SDA_DVFS AC2 SDA_DVFS
VCCA VCCB A1 B1 A2 B2 OE GND
IIC_DVFS_SCL <15>
IIC_DVFS_SDA <15>

AVS(3.3V)

AVS2 AT26 AVS2/GP7_01/PMIC <14,15>
AVS1 AR27 AVS1/GP7_00/PMIC <14,15>
This Level-Shifter is for disconnecting U1 and V3P3 voltage while D3.3V is not supplied.

SYSTEM(1.8V)

AT31 BSMODE_18
AR31 TEST2_18 R43 0 0603
AR32 TEST1_18 R45 0 0603
BSMODE R41 1k 0603 BSMODE_18 <14>
TEST2
TEST1

MLB(3.3V)

MLB_REF H37
C24 10pF 0603 25V
MLB_REF
Bypass Capacitor : 8 pF~10 pF

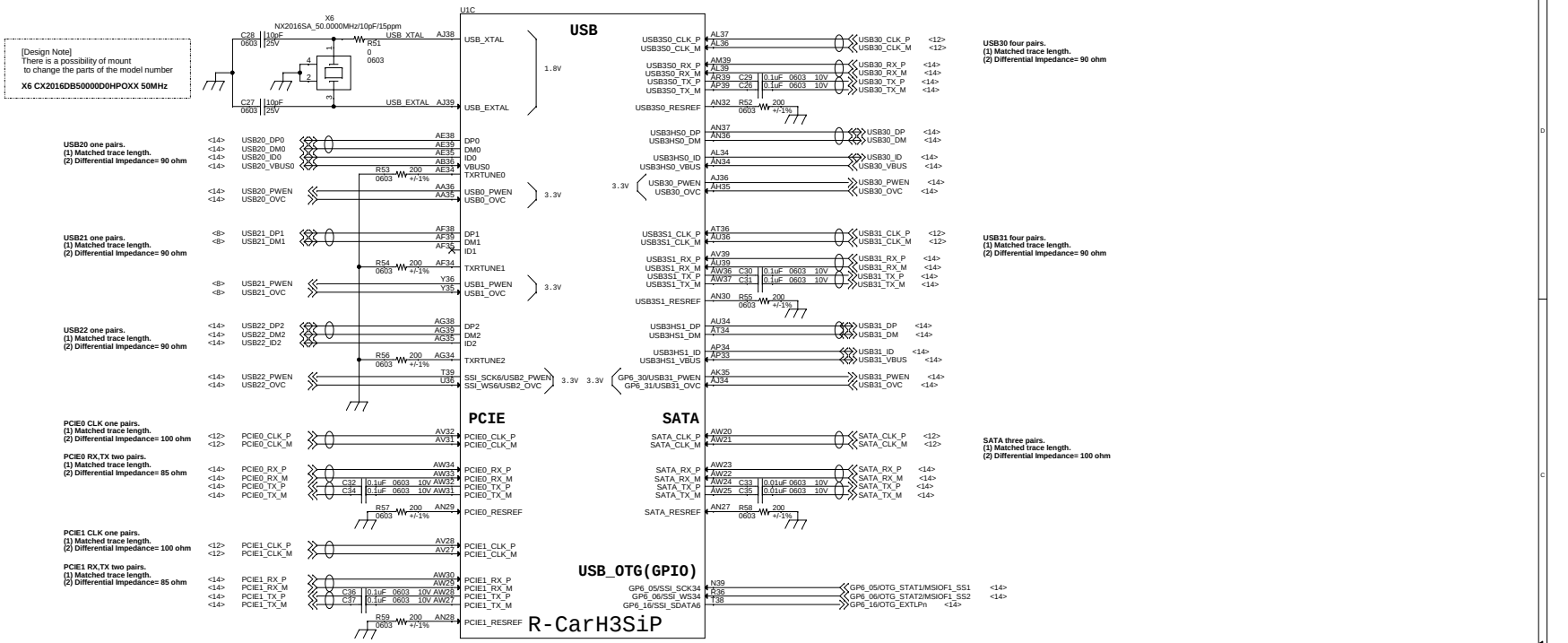
R-CarH3 DU/LBSC

3

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 3 of 15	

Layout Note:
Following signals need Ground guard.

USB_XTAL, USB_EXTAL
GP6_30/INTRQ1 [AUDIO_CLKOUT2_B(50MHz)]
GP6_31/INTRQ2 [AUDIO_CLKOUT3_B(50MHz)]

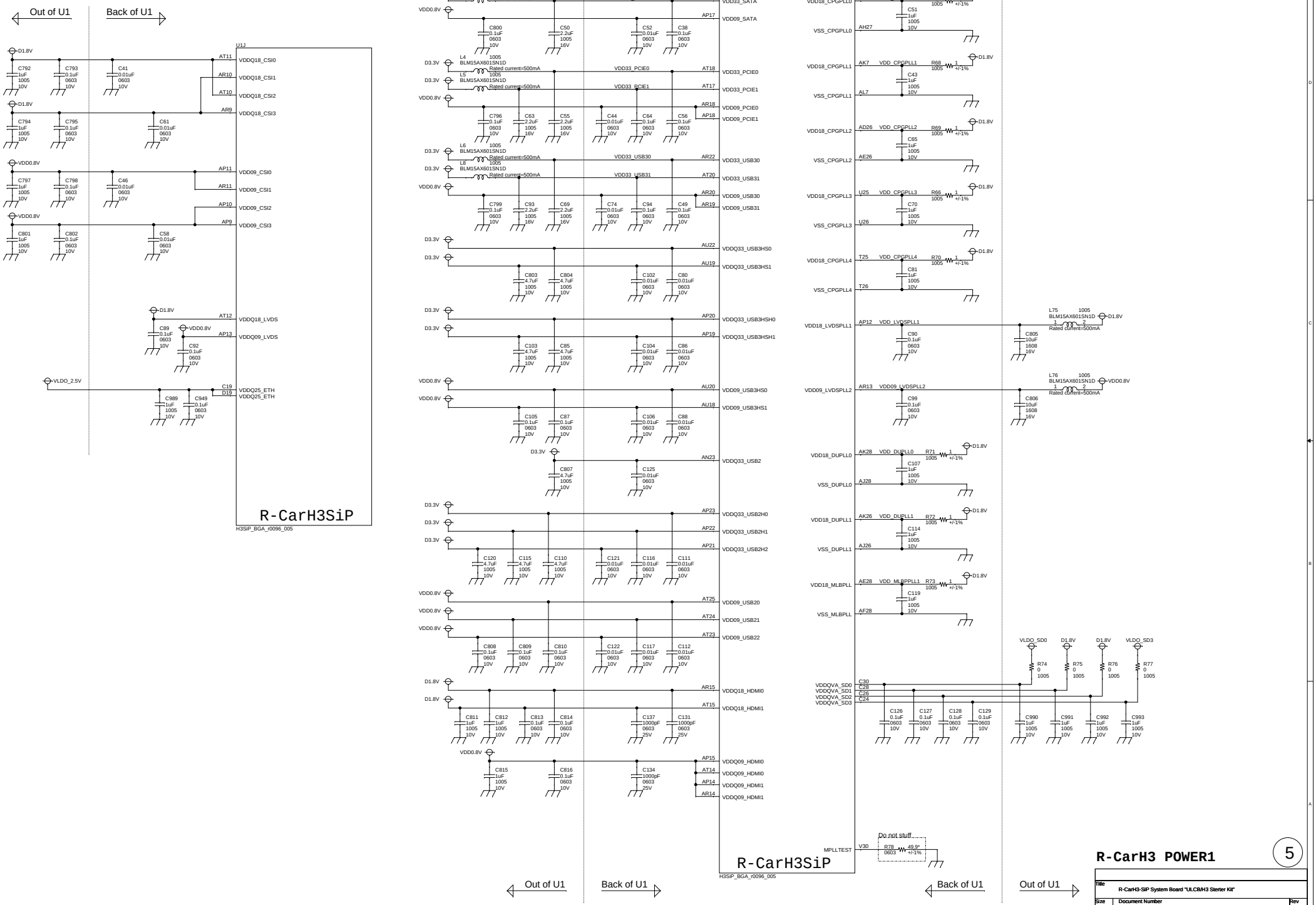


TXRTUNEn (n=0,1,2)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
USB3Sn_RESREF (n=0,1)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
PCIEn_RESREF (n=0,1)
Pull-down(GND) : 200ohm +-1% 100ppm/°C
SATA_RESREF
Pull-down(GND) : 200ohm +-1% 100ppm/°C
CSIn_REXT (n=0-3)
Pull-down(GND) : 4.02kohm
HDMIn_RREF (n=0,1)
Pull-down(GND) : 1620ohm +-1%

R-CarH3 USB/HDMI

4

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 4 of 15	


Out of U1
Back of U1
U1J
U1H
R-CarH3SiP
H3SiP_BGA_r0096_005
D1.8V
VDD0.8V
D3.3V
VLDO_2.5V
VDDQ18_CSI0
VDDQ18_CSI1
VDDQ18_CSI2
VDDQ18_CSI3
VDDQ09_CSI0
VDDQ09_CSI1
VDDQ09_CSI2
VDDQ09_CSI3
VDDQ18_LVDS
VDDQ09_LVDS
VDDQ25_ETH
VDDQ33_SATA
VDDQ09_SATA
VDDQ33_PCIE0
VDDQ33_PCIE1
VDDQ09_PCIE0
VDDQ09_PCIE1
VDDQ33_USB30
VDDQ33_USB31
VDDQ09_USB30
VDDQ09_USB31
VDDQ33_USB3HS0
VDDQ33_USB3HS1
VDDQ33_USB3HSH0
VDDQ33_USB3HSH1
VDDQ09_USB3HS0
VDDQ09_USB3HS1
VDDQ33_USB2
VDDQ33_USB2H0
VDDQ33_USB2H1
VDDQ33_USB2H2
VDDQ09_USB20
VDDQ09_USB21
VDDQ09_USB22
VDDQ18_HDMI0
VDDQ18_HDMI1
VDDQ09_HDMI0
VDDQ09_HDMI1
VDD18_CPGPLL0
VDD18_CPGPLL1
VDD18_CPGPLL2
VDD18_CPGPLL3
VDD18_CPGPLL4
VDD18_LVDSPLL1
VDD09_LVDSPLL2
VDD18_DUPLL0
VDD18_DUPLL1
VDD18_MLBPPLL
VSS_CPGPLL0
VSS_CPGPLL1
VSS_CPGPLL2
VSS_CPGPLL3
VSS_CPGPLL4
VSS_DUPLL0
VSS_DUPLL1
VSS_MLBPLL
VDDQVA_SD0
VDDQVA_SD1
VDDQVA_SD2
VDDQVA_SD3
MPLLTEST
Do not stuff
R-CarH3 POWER1
R-Car H3 SiP System Board "ULCB/H3 Starter Kit"
Document Number
R-Car H3-SiP System Board "ULCB/H3 Starter Kit"
Rev
1.01
Friday, June 17, 2016
Sheet 5 of 15

```
Capacitor-Pin Combination
D3.3V(VDDQ33)
  C142---J33
  C143---L26
  C144---N27
  C145---N33
  C146---T33
  C147---U28,U29
  C148---W28,W29
  C149---AD25,AE24
  C150---AH5
  C151---AJ27
  C152---AJ5
  C153---AK24
  C154---AM7
  C604---AN25
  C605---AN6
  C606---AP24
  C607---AR16
  =17pcs
```

```
Capacitor-Pin Combination
D1.8V(VDDQ18)
  C157---Y5,AA5
  C158---AD3,AE2,AE3
  C159---AD6,AE6
  C160---AF26,AF27,AG26
  C608---AH6
  C609---AJ10
  C610---AN26
  C611---AP16
  =8pcs
```

U1G

D3.3V

VDD0.8V

D1.8V

DVFS0.8V

R-CarH3SiP

H3SiP_BGA_r0096_005

```
Capacitor-Pin Combination
VDD0.8V(VDD)
  C162---M3
  C163---N5
  C879---R3
  C165---U6
  C880---W27

  C167---AA28
  C881---AD11
  C874-+
  C875-+
  C876-+
  C877-+
  C882---AF13
  C883---AF15
  C171---AF17,AG18
  C172---AF19
  C173---AF21
  C174---AG20
  C175---AG22,AG23
  C884---AH11

  C177---AJ18
  C885---AJ22
  C886---AK11
  C180---AK23
  C887---AN10
  C888---AN12
  C889---AN13
  C890---AN16
  C891---AN18
  C892---AN20
  C893---AN22
  =28-2+4=30pcs
```

[VDD]
Back of U1
=32pcs

VDD0.8V

C162 0.047uF 1005 25V
C163 0.22uF 1005 16V
C879 10uF 1608 16V
C165 0.22uF 1005 16V
C880 0.01uF 0603 10V
C167 0.022uF 1005 50V
C881 0.47uF 1005 35V
C874 0.22uF 1005 16V
C875 0.47uF 1005 35V
C876 2.2uF 1005 16V
C877 2.2uF 1005 16V
C882 0.01uF 0603 10V
C883 0.01uF 0603 10V
C171 4700pF 0603 16V
C172 4700pF 0603 16V
C173 0.01uF 0603 10V
C174 0.01uF 0603 10V
C175 0.01uF 0603 10V

VDD0.8V

C884 0.047uF 1005 25V
C177 0.01uF 0603 10V
C885 0.01uF 0603 10V
C886 0.01uF 0603 10V
C180 0.01uF 0603 10V
C887 0.47uF 1005 35V
C888 0.022uF 1005 50V
C889 0.047uF 1005 25V
C890 0.022uF 1005 50V
C891 0.022uF 1005 50V
C892 0.022uF 1005 50V
C893 0.047uF 1005 25V
C929 0.1uF 0603 10V
C930 0.1uF 0603 10V

```
Capacitor-Pin Combination
DVFS0.8V(VDD_DVFS)
  C863---Y10,Y11,AA10
  C861-+
  C864---Y12,AA12
  C865---Y14
  C862-+
  C878-+
  C866---AA13,AA14
  C867---AB12,AC12
  C195---AB14,AB15
  C868---AC10,AC11
  C869---AC13,AC14,AD14,AD15,AE14
  C198---AD12,AE11,AE12,AF11
  C870---AE10
  C200---AE16
  C201---AE18
  C871---AE21
  C203---AG12
  C204---AG14
  C205---AG16
  C206---AH13,AJ14
  C872---AH15
  C873---AH17,AJ16
  C209---AH19
  C210---AH21
  C211---AJ12,AK13
  C212---AJ20
  C213---AK15
  C214---AK17
  C215---AK19
  C216---AK21
  =27+3=30pcs
```

[VDD_DVFS]
Back of U1
=31pcs

DVFS0.8V

C863 2.2uF 1005 16V
C861 10uF 1608 16V
C864 0.22uF 1005 16V
C865 0.22uF 1005 16V
C862 2.2uF 1005 16V
C878 4.7uF 1005 10V
C866 0.22uF 1005 16V
C867 0.47uF 1005 35V
C195 0.22uF 1005 16V
C868 0.47uF 1005 35V
C869 0.47uF 1005 35V
C198 0.22uF 1005 16V
C870 0.047uF 1005 25V
C200 0.047uF 1005 25V
C201 0.047uF 1005 25V
C871 0.047uF 1005 25V

DVFS0.8V

C203 0.01uF 0603 10V
C204 0.01uF 0603 10V
C205 0.01uF 0603 10V
C206 0.01uF 0603 10V
C872 0.022uF 1005 50V
C873 0.022uF 1005 50V
C209 0.01uF 0603 10V
C210 0.01uF 0603 10V
C211 0.022uF 1005 50V
C212 0.01uF 0603 10V
C213 0.022uF 1005 50V
C214 0.022uF 1005 50V
C215 0.01uF 0603 10V
C216 0.047uF 1005 25V
C1017 10uF 1608 16V

DVFS0.8V

C1016 47uF 10V 2012
C1024 47uF 10V 2012

DVFS0.8V

Do not stuff

C1025 47uF 10V 2012

[VDDQ33]
Back of U1
=17pcs

D3.3V

C142 0.1uF 0603 10V
C143 0.1uF 0603 10V
C144 0.1uF 0603 10V
C145 0.1uF 0603 10V
C146 0.1uF 0603 10V
C147 0.1uF 0603 10V
C148 0.1uF 0603 10V
C149 0.1uF 0603 10V
C150 0.1uF 0603 10V
C151 0.1uF 0603 10V
C152 0.1uF 0603 10V
C153 0.1uF 0603 10V
C154 0.1uF 0603 10V
C604 0.1uF 0603 10V
C605 0.1uF 0603 10V
C606 0.1uF 0603 10V
C607 0.1uF 0603 10V

D3.3V

C155 10uF 1608 16V
C156 10uF 1608 16V

[VDDQ18]
Back of U1
=8pcs

D1.8V

C157 0.1uF 0603 10V
C158 0.1uF 0603 10V
C159 0.1uF 0603 10V
C160 0.1uF 0603 10V
C608 0.1uF 0603 10V
C609 0.1uF 0603 10V
C610 0.1uF 0603 10V
C611 0.1uF 0603 10V

D1.8V

C161 10uF 1608 16V

R-CarH3_Sip socket hole is connected to GND.

SKT1
SIP_SOCKET_HOLE

SIP

U1I

TEST_VDDQ
TEST_MON1
TEST_MON2

R-CarH3SiP

H3SiP_BGA_r0096_005

U1F

R-CarH3SiP

H3SiP_BGA_r0096_005

R-CarH3 POWER2

6

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"		
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"		Rev 1.01
Date: Friday, June 17, 2016	Sheet 6 of 15		

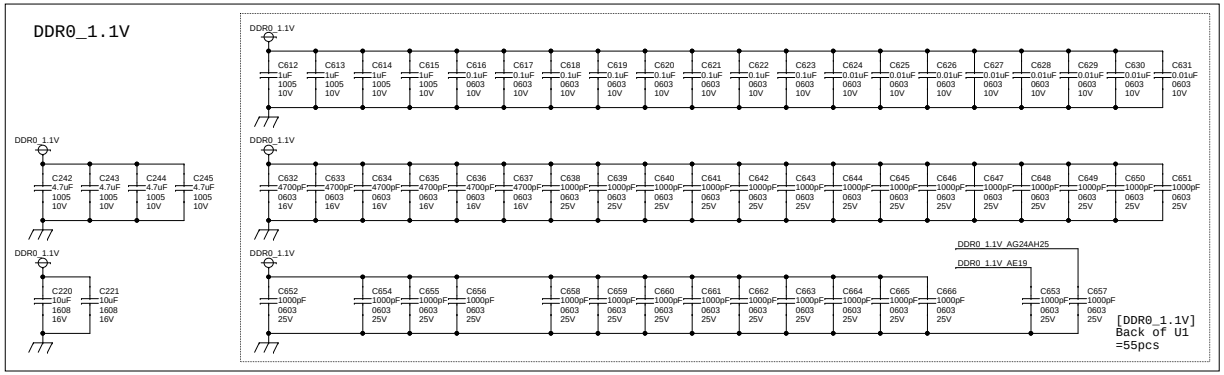
Capacitor-Pin Combination
DDR0_1.1V(VDDQVA_DDR0)
C612---B34,C34
C613---C32
C614---C36
C615---D28
C616---D34
C617---D37
C618---E30,E32
C619---E34
C620---E36
C621---F28
C622---F32
C623---G28
C624---G30
C625---G34
C626---G36
C627---H36
C628---K28,L28
C629---K36
C630---L30
C631---L34
C632---L36,M36
C633---M34
C634---N29
C635---N36
C636---P30
C637---P34
C638---P36
C639---R34
C640---R35
C641---T30
C642---T35
C643---W35
C644---Y30,AA29
C645---Y33,AA33
C646---Y34,AA34
C647---Y37
C648---AC30
C649---AC34
C650---AC36
C651---AD28
C652---AD34,AD35
C653---AE19
C654---AE29
C655---AE30
C656---AE36
C657---AG24,AH25
C658---AG29,AG30
C659---AG36,AH36
C660---AH37
C661---AJ33
C662---AK29
C663---AK34
C664---AL33
C665---AM34
C666---AN31
=55pcs

Capacitor-Pin Combination
DDR0_1.8V(VDD1_M0/M1)
C268---F31
C269---F35
C270---M30
C271---M33
C734---AC29
C735---AC35
C736---AJ30
C740---AJ35
=8pcs

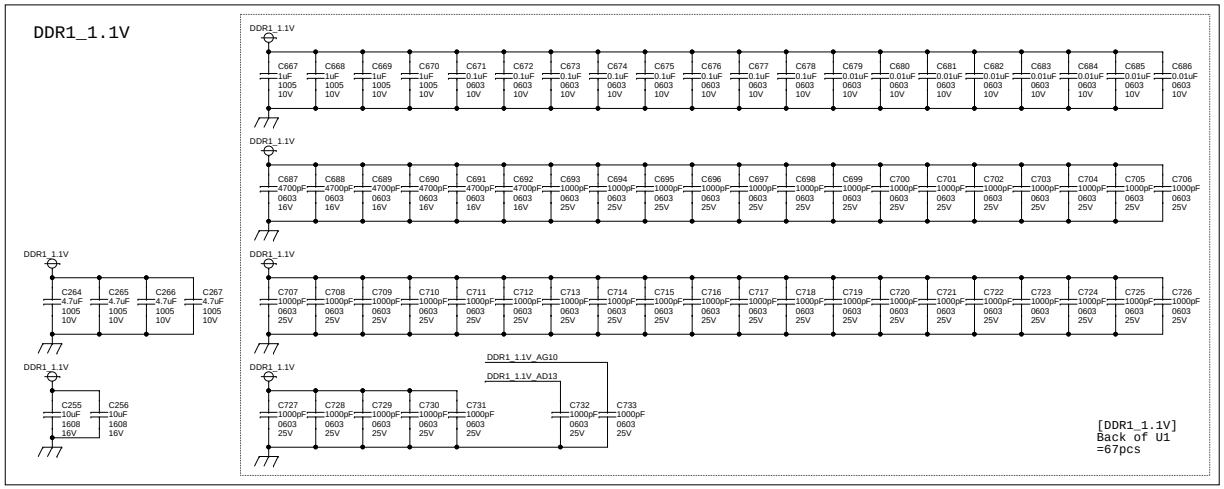
Capacitor-Pin Combination
DDR1_1.8V(VDD1_M2/M3)
C272---F8
C273---F10
C274---F19
C275---F23
C737---M7
C738---M10
C739---M19
C741---M23
=8pcs

Capacitor-Pin Combination
DDR1_1.1V(VDDQVA_DDR0)
C667---C8
C668---C8
C669---C10
C670---C18
C671---D5
C672---D8
C673---D10
C674---D13
C675---D16
C676---D22,E22
C677---E6
C678---E8
C679---E10
C680---E12
C681---E18
C682---E24,D25
C683---F13
C684---F16
C685---F20
C686---F25
C687---G4
C688---G8
C689---G10,G11
C690---G13
C691---G16
C692---G18
C693---G22
C694---G24,G25
C695---H4
C696---H6
C697---K4
C698---K6
C699---K11
C700---K13
C701---K16
C702---K18
C703---K24
C704---K25
C705---L4
C706---L5,M6
C707---L7
C708---L10
C709---L13
C710---L16
C711---L18,M18
C712---L20
C713---L22,M22
C714---L25
C715---M12
C716---M24
C717---N13,P13
C718---N18,P18
C719---P10
C720---P16
C721---P20
C722---P22
C723---P25
C724---P4,R5
C725---P7,R6,R7
C726---R10
C727---R11,R12
C728---R18
C729---R20
C730---R22
C731---R24
C732---AD13
C733---AG10
=67pcs

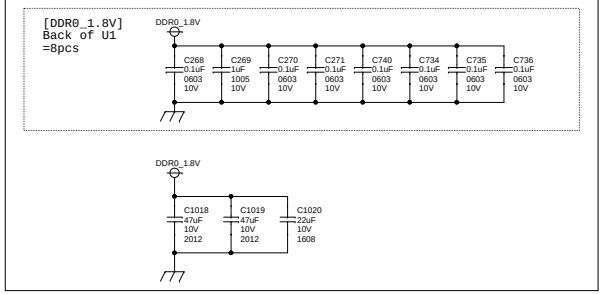
DDR0_1.1V



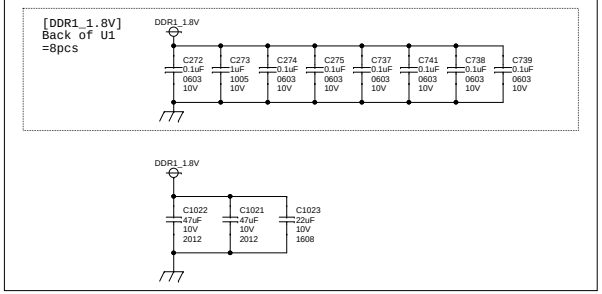
DDR1_1.1V

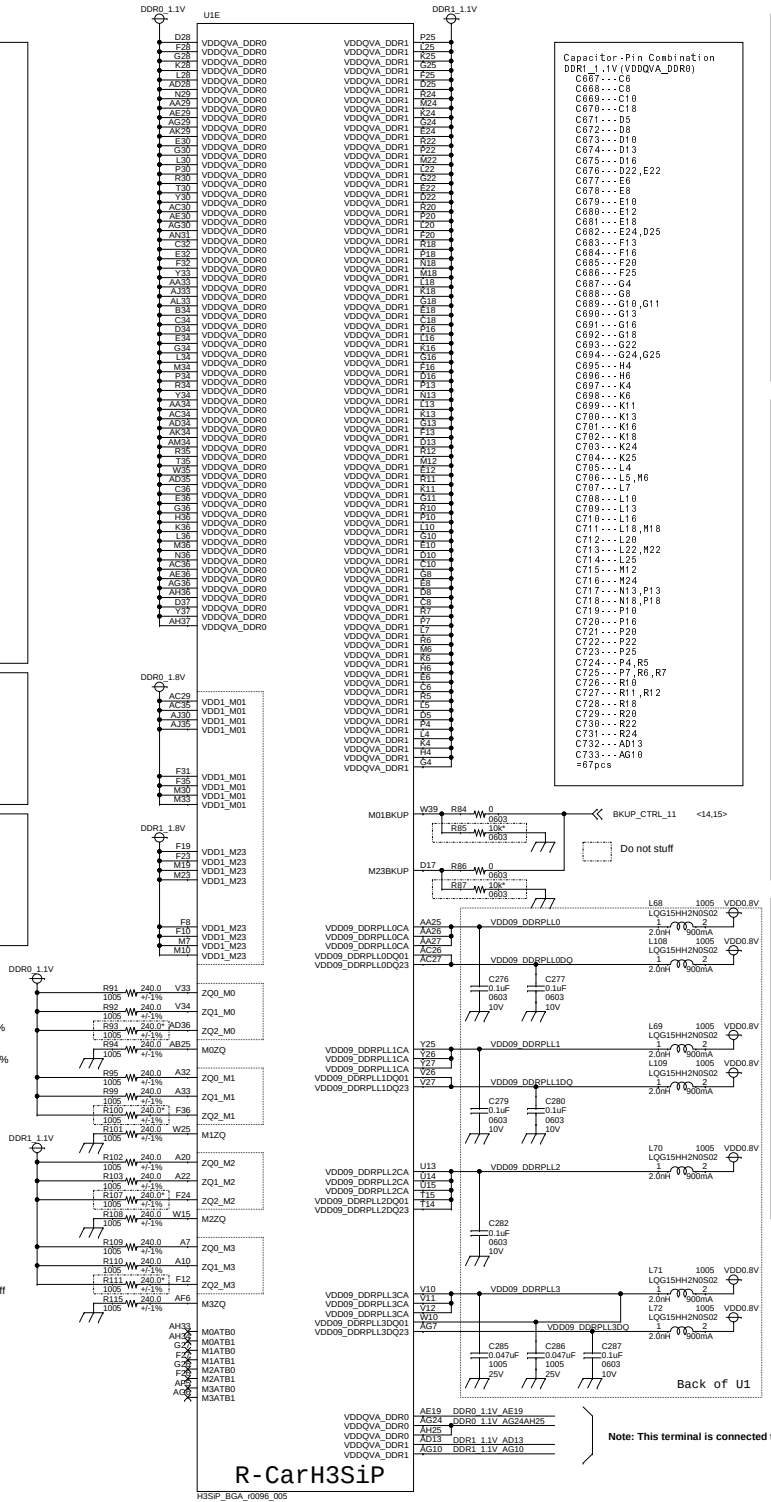


DDR0_1.8V



DDR1_1.8V





R-CarH3 LPDDR_POWER

7

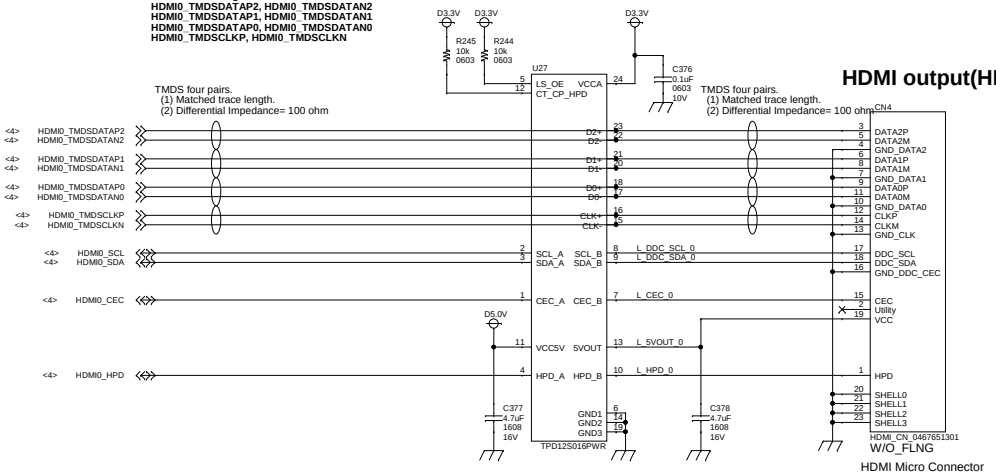
Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 7 of 15	

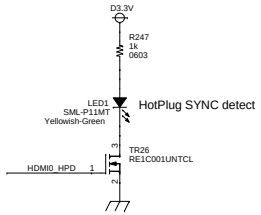
Layout Note:

Matched trace length from SoC until CN16
HDMI0_TMDSDATAP2, HDMI0_TMDSDATAN2
HDMI0_TMDSDATAP1, HDMI0_TMDSDATAN1
HDMI0_TMDSDATAP0, HDMI0_TMDSDATAN0
HDMI0_TMDSCLKP, HDMI0_TMDSCLKN

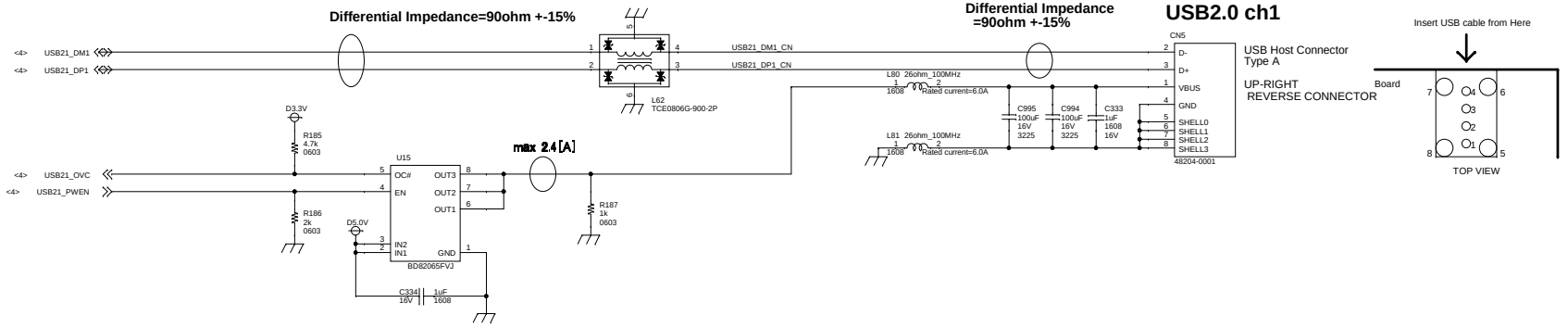
HDMI COMPANION CHIP
WITH ESD PROTECTION, I2C LEVEL SHIFTER

HDMI output(HDMI0)



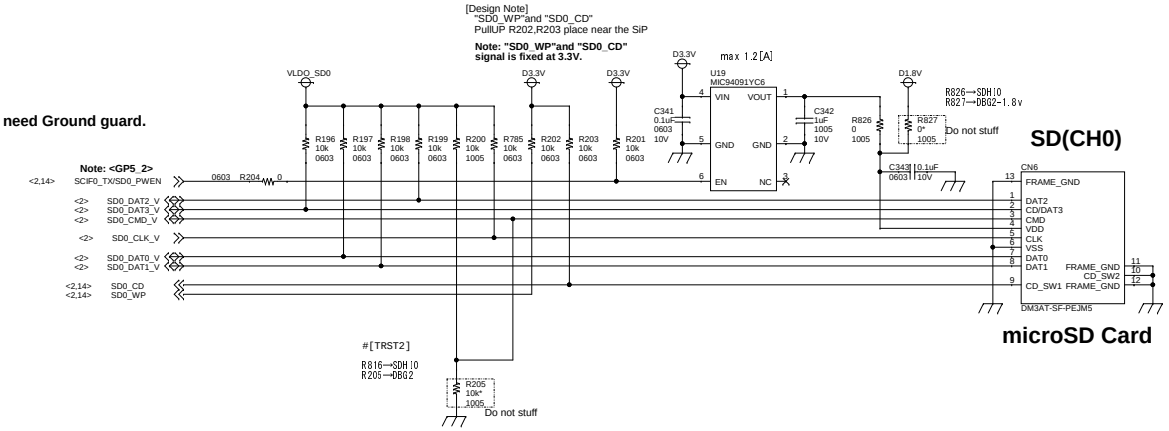


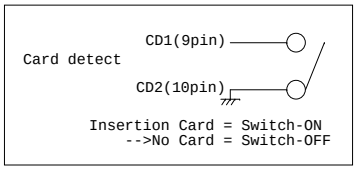
USB2.0 ch1



SD(CH0)

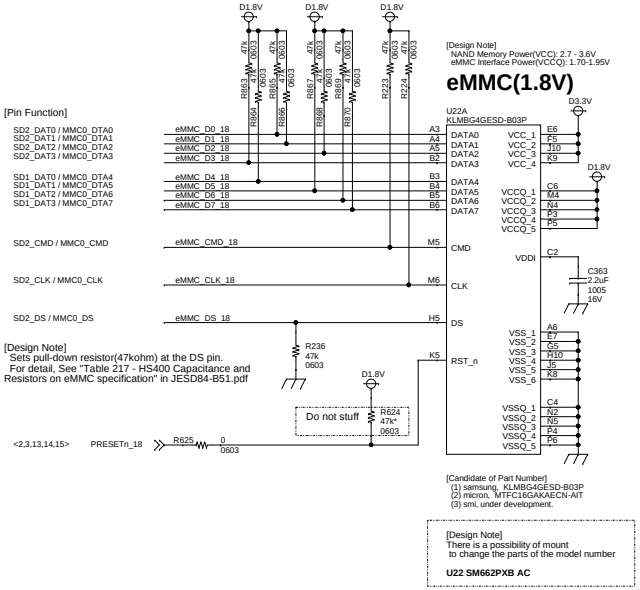
Layout Note:
Following signals need Ground guard.
SD0_CLK_V

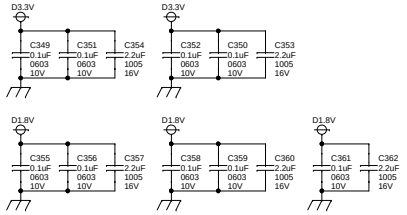


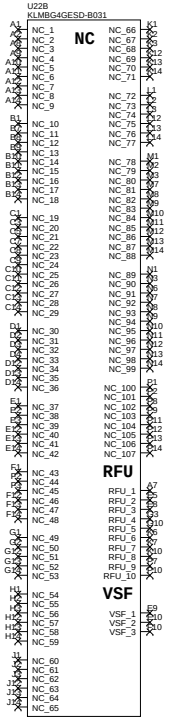


HDMI_OUT/USB2.0/SDHI0 8

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 8 of 15	







Layout Note:
Following signals need Ground guard.

MMC0_CLK_V, eMMC_CLK_18

Layout Note:
Matched Trace Length from R-CarH3-SiP to eMMC. max 400Mbps/pin

Group 1
MMC0_DTA[7:0]_V + eMMC_D[7:0]_18
MMC0_CMD_V + eMMC_CMD_18
MMC0_CLK_V + eMMC_CLK_18
MMC0_DS_V + eMMC_DS_18

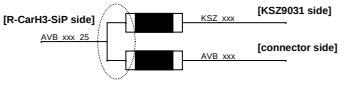
MMC0

9

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"		
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"		Rev 1.01
Date: Friday, June 17, 2016	Sheet 9 of 15		

Ethernet AVB GbPHY and PHY Connector

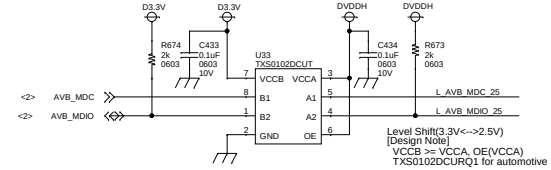
Layout Note:
As short as possible from junction of AVB_xxx to two Rxxx.

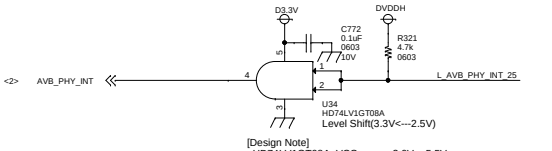


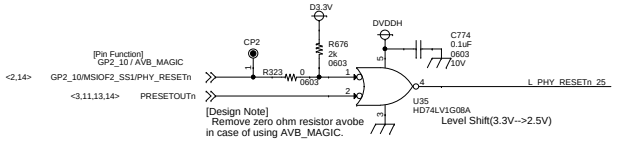
Layout Note:
Matched Trace Length from R-CarH3-Sip to KSZ9031.
(max 250Mbps/pin)
Group 1
AVB_TXC + KSZ_GTX_CLK
AVB_TX_CTL+KSZ_TX_EN
AVB_TD[3:0] + KSZ_TXD[3:0]
Group 2
AVB_RXC + KSZ_RX_CLK
AVB_RX_CTL + KSZ_RX_DV
AVB_RD[3:0] + KSZ_RXD[3:0]

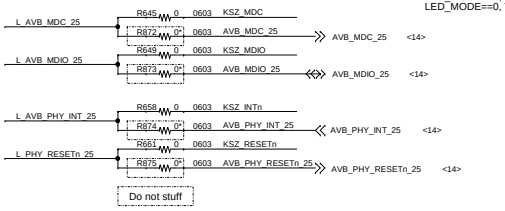
Layout Note:
Following signals need Ground guard.
AVB_TXCREFCLK (125MHz)
AVB_TXC_25, KSZ_GTX_CLK, EX_GTX_CLK (125MHz)
AVB_RXC_25, KSZ_RX_CLK, EX_RX_CLK (125MHz)

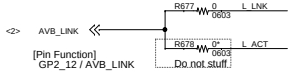
Following pin has pull-down resistor at the initial state.
[2.5V-I/O]
AVB_RX_CTL, AVB_RXC, AVB_RD[3:0]
AVB_TX_CTL, AVB_TXC, AVB_TD[3:0]
[3.3V-I/O]
AVB_TXCREFCLK, AVB_MAGIC, AVB_PHY_INT, AVB_LINK

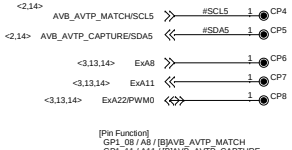








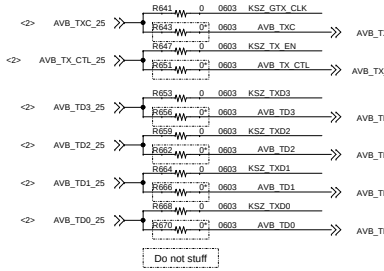


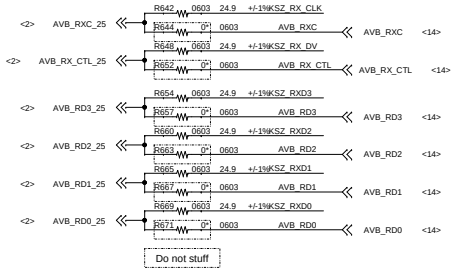


for Ether ComExpress version.

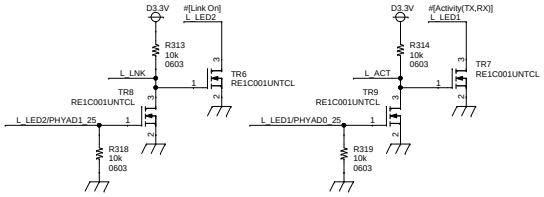
Note:
To make RGMII connection to ComExpress. change below component mount/unmount.

Unmount	Mount	Change value
R642,	C985,	100ohm ->22ohm
R648,	R643,	R724,
R654,	R644,	R725,
R660,	R651,	R726,
R665,	R652,	R727,
R669,	R656,	R728,
R641,	R657,	R729,
R647,	R662,	
R653,	R663,	
R659,	R666,	
R664,	R667,	
R668,	R670,	
R645,	R671,	
R649,	R872,	
R658,	R873,	
R661	R874,	
	R875	

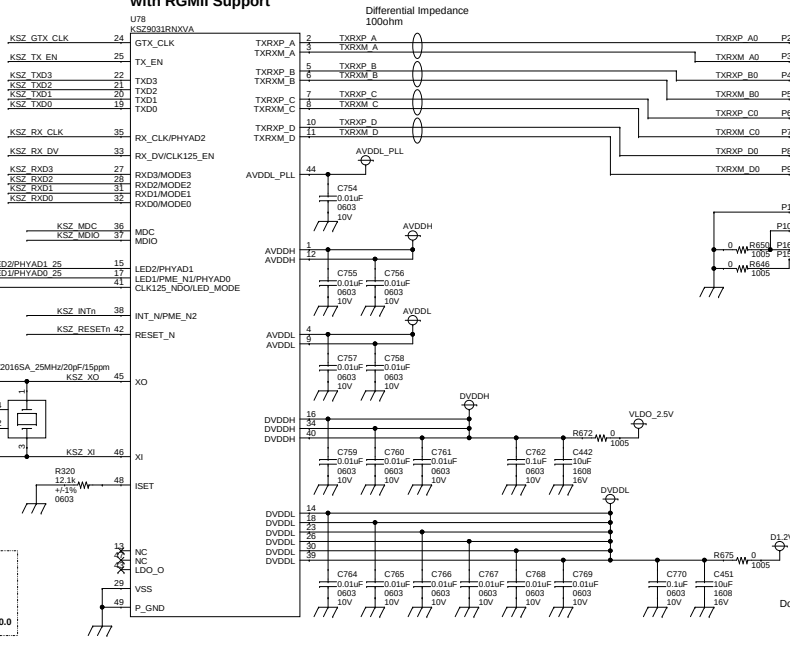




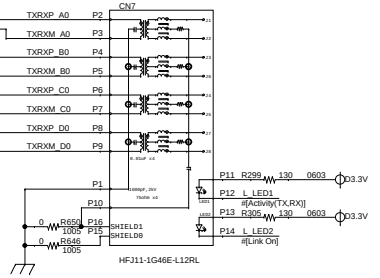
Controls LEDs in the RJ45 connector



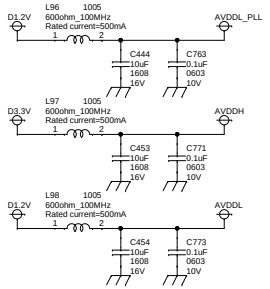
Gigabit Ethernet Transceiver with RGMII Support

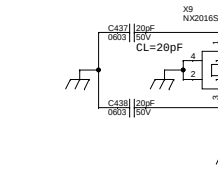


RJ45 with integrated magnetics



LC filters for KSZ9031RNX





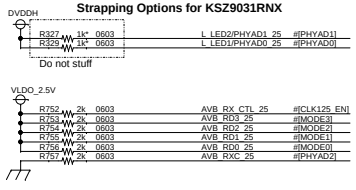
[Design Note]
There is a possibility of mount
to change the parts of the model number

U78 KLMBG4GESD-B03P

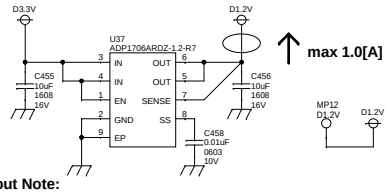
X9 FA-128 25.000000 MHz 20.0 +10.0-10.0

Layout Note:
The KSZ9031RNX has Paddle Ground (pin49) at bottom side.
Connect that PAD(pin 49) to the GND.

Strapping Options for KSZ9031RNX



Local Regulator for KSZ9031RNX, PHY Connector



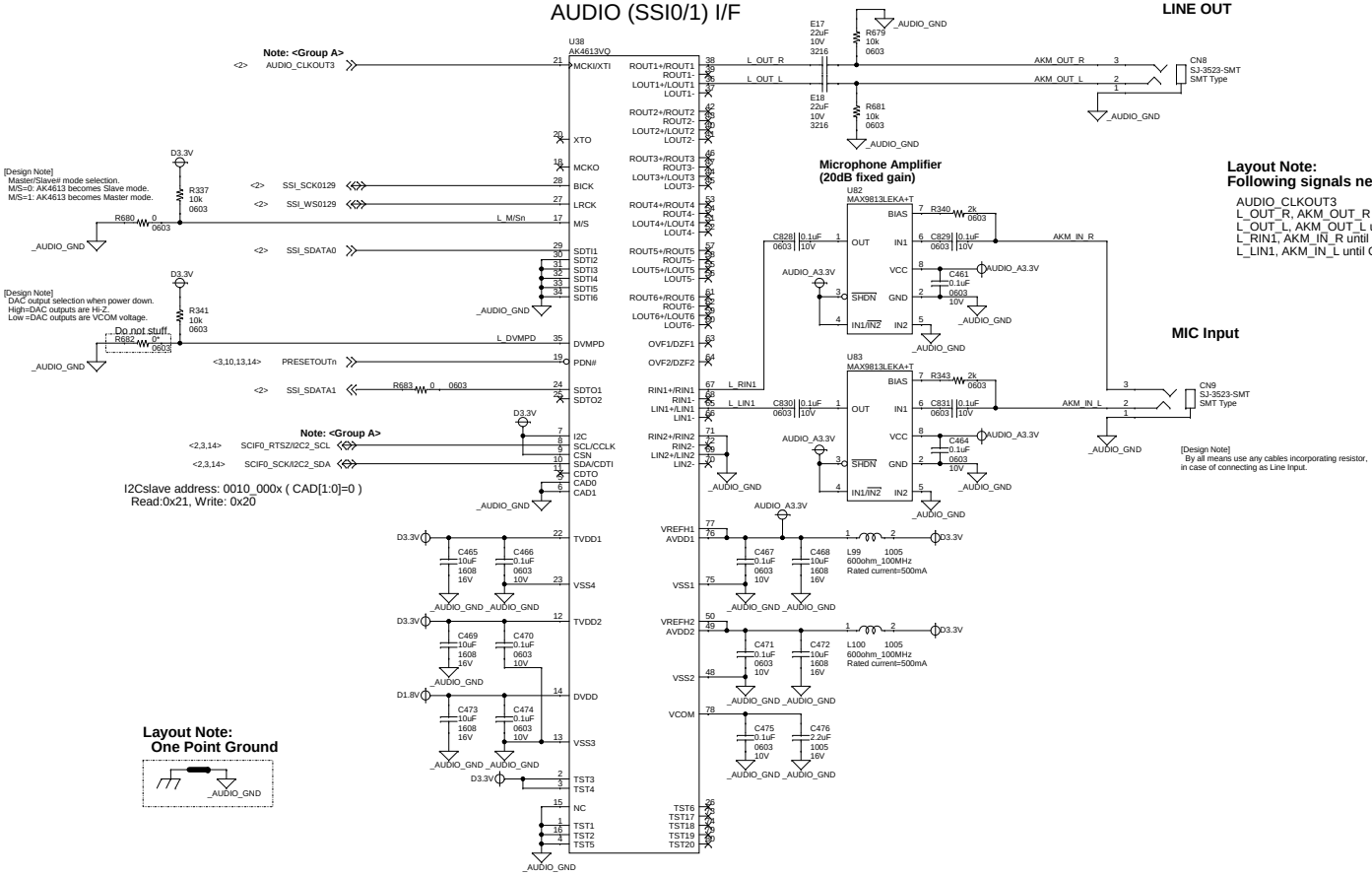
Layout Note:
The ADP1706 has EXPOSED PAD(pin9) at bottom side.
Connect that EXPOSED PAD(pin 9) to the GND.

EtherAVB(GbPHY)

10

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 10 of 15	

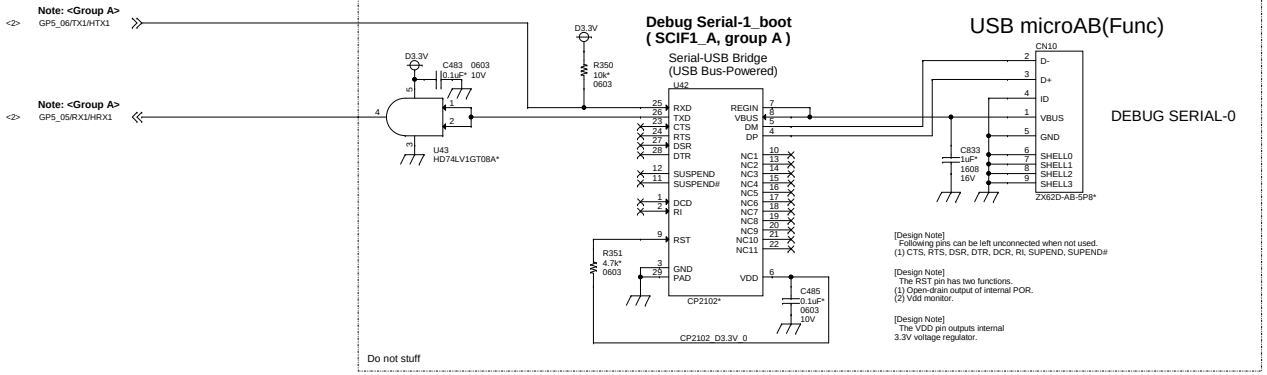
AUDIO (SSI0/1) I/F



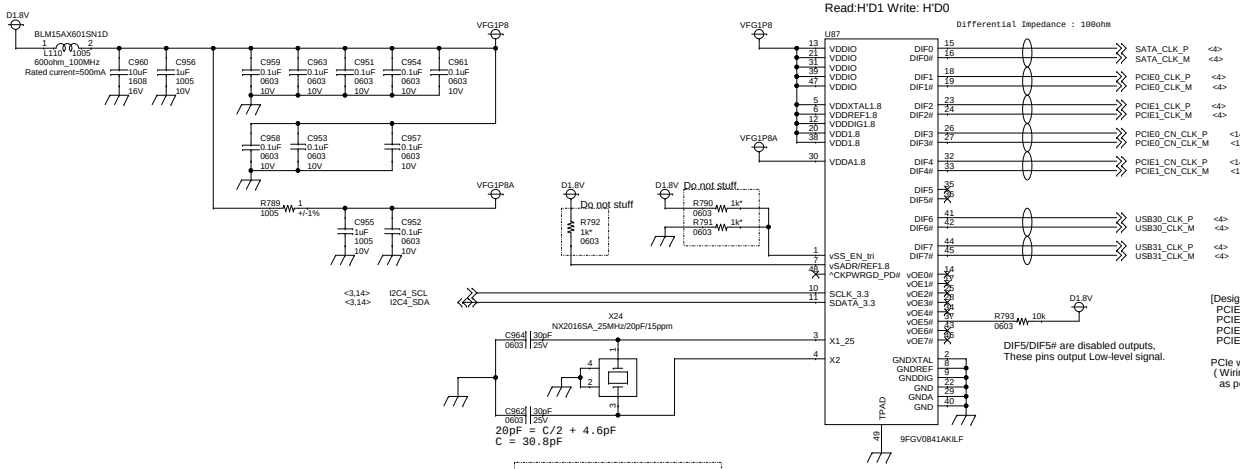
AUDIO(AK4613VQ)

11

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 11 of 15	



I2Cslave address: 1101_000X
Read:H'D1 Write: H'D0



[Design Note]
There is a possibility of mount
to change the parts of the model number

X24 FA-128 25.000000 MHz 20.0 +10.0-10.0

v : prefix indicates internal 120KOhm pull down resistor
^ : prefix indicates internal 120KOhm pull up resistor

Power Management Table

CKPWRGD_PD#	SMBus OE bit	DIFx OEx#	DIFx True O/P	DIFx Comp. O/P	REF
0	X	X	Low	Low	Hi-Z
1	1	0	Running	Running	Running
1	0	1	Low	Low	Low

SMBus Address Selection Table (I2C Slave address)

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

Select Spread Spectrum Table

vSS_EN_tri	Spread Spectrum
0	Spread Off
M	-0.25%
1	-0.5%

'M' is Mid Voltage = 0.5VDD = 0.9V.
This setting can be controled by software.
Refer to datasheet chapter of "SMBus Table : SS Readback and Control Register"

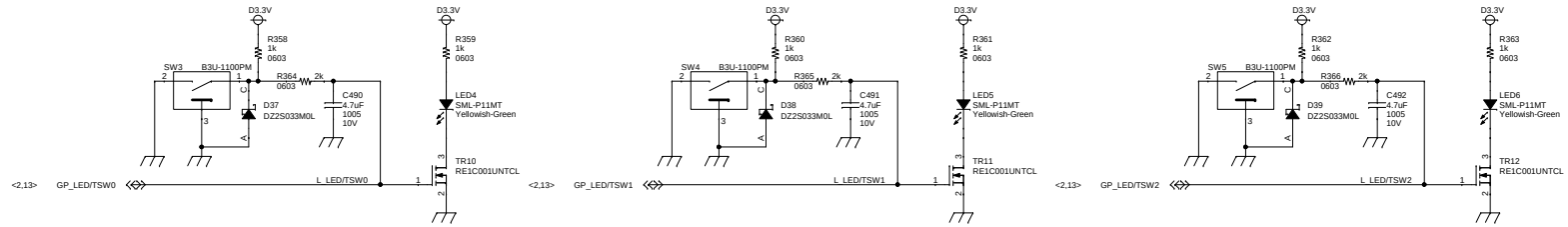
DIF5/DIF5# are disabled outputs,
These pins output Low-level signal.

[Design Note]
PCIE0_CLK_P , PCIE0_CLK_M
PCIE1_CLK_P , PCIE1_CLK_M
PCIE0_CN_CLK_P , PCIE0_CN_CLK_M
PCIE1_CN_CLK_P , PCIE1_CN_CLK_M

PCIe wiring from the Clock generator to longer wiring on the ULCB side
(Wiring to the ULCB -side device and ComExpress of previous devices
as possible to the same length)

GPLED / Tact Switch

General Purpose LEDs or Tactile Switches
Following LEDs and Switches are connected to GPIO of R-CarH3-SiP



DEBUG_SCIF/Clock_Gen/LED/TactSW

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 12 of 15	

Layout Note:
Following signals need Ground guard.

CPLDCLK
BS1_TCK

[Design Note]
There is a possibility of mount
to change the parts of the model number

X25 SG-210SCB 22.5792MHz L

D3.3V CPLD Reference Clock

SERIES_TERM

C1008 0.1uF 0603 10V

X25 VCC OUT STn GND

NZ2520SB_22.5792MHz/50ppm

R794 0 0603

List of CPLD Functions

Local Bus State Controller(LBSC_D)
>>> ExD0...
Local Bus State Controller(LBSC_A/DU)
>>> ExA0...
Local Bus State Controller(LBSC/DU)
Clock-Synchronized Serial Interface(MSIOF)
QSPI Select SW Signal
>>> QSPI_CPLDSW
Reset Signal for H3 SoC [PRESETn_18 signal level conversion]
>>> PRESETn_33
PMIC Manual Reset Signal
>>> PRESET_SYSZ_PMIC
Reset Signal [From LUCY]
>>> PRESET_SYSZ
Mode setting Signal
>>> Mode_Pin0...
BKUP_REQB
>>> Back Up Set Up Finish Signal
Back Up Setup Start Signal [SDRAM Backup Signal]
>>> BKUP_TRG , SYS_TRG
BOOST
>>> DVFS Boost Signal
DVFS_PGD
>>> DVFS Power Good Signal
CPLD Reset Signal
>>> PRESETOUTn
CPLD Reference Clock
>>> CPLDCLK
LED/Tact Switch
>>> L_LED/TSW0...
PWM

Mode Setting CPLD

U88 — 5M240ZM100

ExA15	B1	IO_B1[1]	
CF_MaX2	C2	IO_B1[2]	
ExA14	C1	IO_B1[3]	
ExA25/PWM4	D3	IO_B1[4]	
CF_MaX1	D2	IO_B1[5]	
ExA18	D1	IO_B1[6]	
Mode_Pin3	E2	IO_B1[7]	
CPLDCLK	F2	IO_B1[8]/CLK0	
ExA19	E1	IO_B1[9]/CLK1	
ExA17	F1	IO_B1[10]	
Mode_Pin1	G1	IO_B1[11]	
BS1_TDI	G2	IO_B1[12]	
ExA20/PWM2	F3	IO_B1[13]	
Mode_Pin0	H1	IO_B1[14]	
L_LED/TSW0	H3	IO_B1[15]	
Mode_Pin2	H2	IO_B1[16]	
ExD0	L1	IO_B1[17]	
ExD1	L2	IO_B1[18]	
ExA21/PWM1	K3	IO_B1[19]	
ExD3	L3	IO_B1[20]	
L_LED/TSW2	K4	IO_B1[21]	
ExD2	L4	IO_B1[22]	
PUSH_RESET	K5	IO_B1[23]	
ExD5	L5	IO_B1[24]	
ExD4	L6	IO_B1[25]	
DVFS_PGD	J5	IO_B1[26]	
GP6_08	MSIOF1_SCK/SSI_SCK4	K6	IO_B1[27]
BKUP_REQB	J6	IO_B1[28]	
ExD7	L7	IO_B1[29]	
	K7	IO_B1[30]	
ExD6	L8	IO_B1[31]	
PRESETOUTn	K8	IO_B1[32]/DEV_OE	
ExD9	L9	IO_B1[33]/DEV_CLRn	
	K9	IO_B1[34]	
ExD8	L10	IO_B1[35]	
QSPI_CPLDSW	K10	IO_B1[36]	
ExD11	L11	IO_B1[37]	
		IO_B1[38]	

	K11	IO_B2[1]	ExD10
	J10	IO_B2[2]	PRESETn_33
	J11	IO_B2[3]	ExD13
	H9	IO_B2[4]	BKUP_TRG
	H10	IO_B2[5]	PRESET_SYSZ_PMIC
	H11	IO_B2[6]	ExD12
	G10	IO_B2[7]	MSIOF1_TXD/LVDS_BLEN GP6_07
	F9	IO_B2[8]	L_LED/TSW1
IO_B2[9]/CLK2	F10		CS0n
IO_B2[10]/CLK3	G11		ExD15
	F11	IO_B2[11]	ExD14
	E11	IO_B2[12]	ExA1
	E10	IO_B2[13]	HIZ_TXD
	D9	IO_B2[14]	PWM1
	D11	IO_B2[15]	ExA0
	D10	IO_B2[16]	MSIOF1_SYNC/SSI_WS4 GP6_09
	C11	IO_B2[17]	ExA3
	C10	IO_B2[18]	MSIOF1_RXD/SSI_SDATA4 GP6_10
	B11	IO_B2[19]	ExA2
	B10	IO_B2[20]	PRESET_SYSZ
	A11	IO_B2[21]	ExA5
	A10	IO_B2[22]	ExA4
	B9	IO_B2[23]	ExA16
	A9	IO_B2[24]	ExA7
	B8	IO_B2[25]	RD/WR#/GP1_24/CAN0_RX
	A8	IO_B2[26]	ExA6
	B7	IO_B2[27]	ExA23/DU_EXVSYNC_DU_VSYNC
	A7	IO_B2[28]	ExA9
	C6	IO_B2[29]	PWM2
	B6	IO_B2[30]	MDT1/RDn/GP1_23/CAN0_TX
	C7	IO_B2[31]	SYS_TRG
	A6	IO_B2[32]	ExA8
	C5	IO_B2[33]	BOOST
	A5	IO_B2[34]	ExA11
	B5	IO_B2[35]	MDT0/BSn/GP1_22/CAN1_TX
	A4	IO_B2[36]	ExA10
	B4	IO_B2[37]	BS1_TMS
	A3	IO_B2[38]	ExA13
	B3	IO_B2[39]	ExA24/DU_EXHSYNC_DU_HSYNC
	A2	IO_B2[40]	ExA12
	B2	IO_B2[41]	ExA22/PWM0

J1 TMS, K1 TCK, J2 TDI, K2 TDO

CP9, CP10, CP11

BS1_TDO — R795 33 0603 — BS_TMS
BS1_TMS — R796 33 0603 — BS_TCK
BS1_TDI — R797 33 0603 — BS_TDI

CN11 — PSS-710153-06 1.27mm PinHeader

SW7 SKRPABE010 — R861 10k 0603 — PUSH_RESET — C1026 0.1uF 0603 10V

BKUP_REQB — R615 2k 0603

U121 SN74AUP1T34DCK — PRESETn_18 — PRESETn_33 — Level Shift(1.8V ---> 3.3V)

C1010 0.1uF 0603 10V
C1009 0.1uF 0603 10V

C965–C970 0.1uF 0603 10V
C971–C972 0.1uF 0603 10V

[Design Note]
Signal connected only to CPLD

PRESET_SYSZ_PMIC , CPLDCLK , Mode_Pin0-3 , QSPI_CPLDSW , BOOST

Debug Serial-0_consol
(SCIF2_A, group A)

<2> SCIF2_TXD — R884 10k 0603 — RXD
<2> SCIF2_RXD — C1027 0.1uF 0603 10V — U123 HD74LV1GT08A — TXD

CF_MaX1 — BS_TMS — R841 0603 0 — RTS*
CTS*
CF_MaX2 — BS_TCK — R842 0603 0 — DTR#
DSR#
BS_TDI — R843 0603 0 — DCD#
BS1_TDO — R844 0603 0 — RI#

U122 FT232RQ — 3V3OUT — VCCIO — VCC — USBDM — USBDP — OSCI — OSCO — RESET# — R845 10k 0603 — HIZ_TXD — CBUS0–CBUS4 — NC — TEST — AGND — GND — H-pad

CN12 ZX62D-AB-5P8 — D- — D+ — ID — VBUS — GND — SHELL0–SHELL3 — VCC5U

C1014 0.1uF 0603 10V
C1013 0.1uF 0603 10V
C1012 0.1uF 16V 1005
C1011 1uF 1608 16V
C1015 0.1uF 0603 10V

Mode setting Signal — SW6 CHS-04A — Mode_Pin0–Mode_Pin3

CN1 : COM Express Connector
U1 : R-CarH3 SiP
U72 : PMIC BD9571MWV-M
U88 : CPLD 5M240ZM100
U89 : BUS SWITCH SN74CB3Q3245RGYR

Local Bus State Controller(LBSC_D) — ExD[0..15] <3,14>

ExD15	CN1.C35 CN1.C92	U1.R1 U88.G11
ExD14	CN1.C34 CN1.C91	U1.R2 U88.F11
ExD13	CN1.C25 CN1.C89	U1.T1 U88.J11
ExD12	CN1.C23 CN1.C88	U1.T2 U88.H11
ExD11	CN1.C27 CN1.C86	U1.U1 U88.L11
ExD10	CN1.C26 CN1.C85	U1.U2 U88.K11
ExD9	CN1.C29 CN1.C83	U1.V1 U88.L9
ExD8	CN1.C28 CN1.C82	U1.V2 U88.L10
ExD7	CN1.B22	U1.W1 U88.L7
ExD6	CN1.C30	U1.W2 U88.L8
ExD5	CN1.B24	U1.Y1 U88.L5
ExD4	CN1.B23	U1.Y2 U88.L6
ExD3	CN1.B25	U1.AA1 U88.L3
ExD2	CN1.B27	U1.AA2 U88.L4
ExD1	CN1.B28	U1.AB2 U88.L2
ExD0	CN1.B25	U1.AB1 U88.L1

Local Bus State Controller(LBSC_A/DU)

ExA25/PWM4	<3,14>	CN1.B62	U1.A4 U88.D3
ExA24/DU_EXHSYNC_DU_HSYNC	<3,14>	CN1.D97	U1.A3 U88.B3
ExA23/DU_EXVSYNC_DU_VSYNC	<3,14>	CN1.D98	U1.B3 U88.B7
ExA22/PWM0	<3,10,14>	CN1.B48 CP8.1	U1.B8 U88.B2
ExA21/PWM1	<3>		U1.B6 U88.K3
ExA20/PWM2	<3,14>	CN1.B44	U1.A6 U88.F3

ExA[0..19] <3,10,14>

ExA19	CN1.D43 CN1.D89	U1.E1 U88.E1
ExA18	CN1.D35 CN1.D88	U1.E2 U88.D1
ExA17	CN1.D38 CN1.D86	U1.E3 U88.F1
ExA16	CN1.C53 CN1.D85	U1.F3 U88.B9
ExA15	CN1.D23 CN1.D95	U1.G1 U88.B1
ExA14	CN1.D22 CN1.D94	U1.G2 U88.C1
ExA13	CN1.D55 CN1.D92	U1.H1 U88.A3
ExA12	CN1.D57 CN1.D91	U1.H2 U88.A2
ExA11	CN1.C81 CP7.1	U1.J1 U88.A5
ExA10	CN1.C102	U1.J2 U88.A4
ExA9	CN1.D50	U1.K1 U88.A7
ExA8	CN1.D52 CP6.1	U1.K2 U88.A6
ExA7	CN1.C61 CN1.D83	U1.L1 U88.A9
ExA6	CN1.C58 CN1.D82	U1.L2 U88.A8
ExA5	CN1.C43 CN1.C101	U1.M1 U88.A11
ExA4	CN1.C42 CN1.C99	U1.M2 U88.A10
ExA3	CN1.C39 CN1.C98	U1.N1 U88.C11
ExA2	CN1.C38 CN1.C97	U1.N2 U88.B11
ExA1	CN1.C37 CN1.C95	U1.P1 U88.E11
ExA0	CN1.C36 CN1.C94	U1.P2 U88.D11

Local Bus State Controller(LBSC/DU)

CS0n	<3,14>	CN1.B46	U1.C2 U88.F10
MDT0/BSn/GP1_22/CAN1_TX	<3,14>	CN1.B19 CN1.B98	U1.C4 U88.B5
MDT1/RDn/GP1_23/CAN0_TX	<3,14>	CN1.B20 CN1.B99	U1.A2 U88.B6
RD/WR#/GP1_24/CAN0_RX	<3,14>	CN1.B40 U1.D3	U88.B8

Reset Signal for H3 SoC [PRESETn_18 signal level conversion] — PRESETn_18 <2,3,9,14,15> — CN1.A46 CN2.1 CN3.15 R625.2 R818.1 TR21.1 U1.AR28 U72.5 U121.2

CPLD Reset Signal — PRESETOUTn <3,10,11,14> — CN1.B50 R33.2 U1.C1 U35.2 U38.19 U88.K8

PMIC Manual Reset Signal — PRESET_SYSZ_PMIC <15> — SW9.2 U72.51 U88.H10

Reset Signal [From LUCY] — PRESET_SYSZ <14> — CN1.B49 U88.B10

Clock-Synchronized Serial Interface(MSIOF)

GP6_08	MSIOF1_SCK/SSI_SCK4	<2,14>	CN1.A79 U1.P39 U88.K6
GP6_09	MSIOF1_SYNC/SSI_WS4	<2,14>	CN1.A71 U1.T37 U88.D10
GP6_07	MSIOF1_TXD/LVDS_BLEN	<2,14>	CN1.B55 U1.N37 U88.G10
GP6_10	MSIOF1_RXD/SSI_SDATA4	<2,14>	CN1.B81 U1.P38 U88.C10

PWM — PWM1 <14> — PWM2 <14,15> — CN1.C30 U88.D9 — CN1.A14 U72.66 U88.C6

Back Up Setup Start Signal [SDRAM Backup Signal] — BKUP_TRG <14,15> — SYS_TRG <14> — CN1.A4 U72.64 U88.H9 — CN1.B62 U88.C7

BKUP_REQB[Back Up Set Up Finish Signal] — BKUP_REQB <14,15> — CN1.A5 R615.2 U72.65 U88.J6

BOOST[DVFS Boost Signal] — BOOST <15> — U72.67 U88.C5

DVFS_PGD[DVFS Power Good Signal] — DVFS_PGD <14,15> — CN1.A6 R508.1 TR13.1 U72.26 U88.J5

QSPI Select SW Signal — QSPI_CPLDSW <2> — R825.1 U88.K10 U89.19

LED/Tact Switch Signal

L_LED/TSW0	GP_LED/TSW0	<2,12>	C490.2 R364.2 TR10.1 U1.R39 U88.H3
L_LED/TSW1	GP_LED/TSW1	<2,12>	C491.2 R365.2 TR11.1 U1.R37 U88.F9
L_LED/TSW2	GP_LED/TSW2	<2,12>	C492.2 R366.2 TR12.1 U1.P37 U88.K4

R-CarH3 MODE Setting

13

Title	R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Starter Kit"	Rev 1.01
Date: Friday, June 17, 2016	Sheet 13 of 15	

Layout Note:
Following signals need Ground guard.

Matched trace length and Differential Impedance

CN1A
401-55501-51

CoM Express A Side

COM Express 440pin

VCC12V0
ULCB Not use

CN1B
401-55501-51

CoM Express B Side

COM Express 440pin

VCC12V0
ULCB Not use

CN1C
401-55501-51

CoM Express C Side

COM Express 440pin

VCC12V0
ULCB Not use

CN1D
401-55501-51

CoM Express D Side

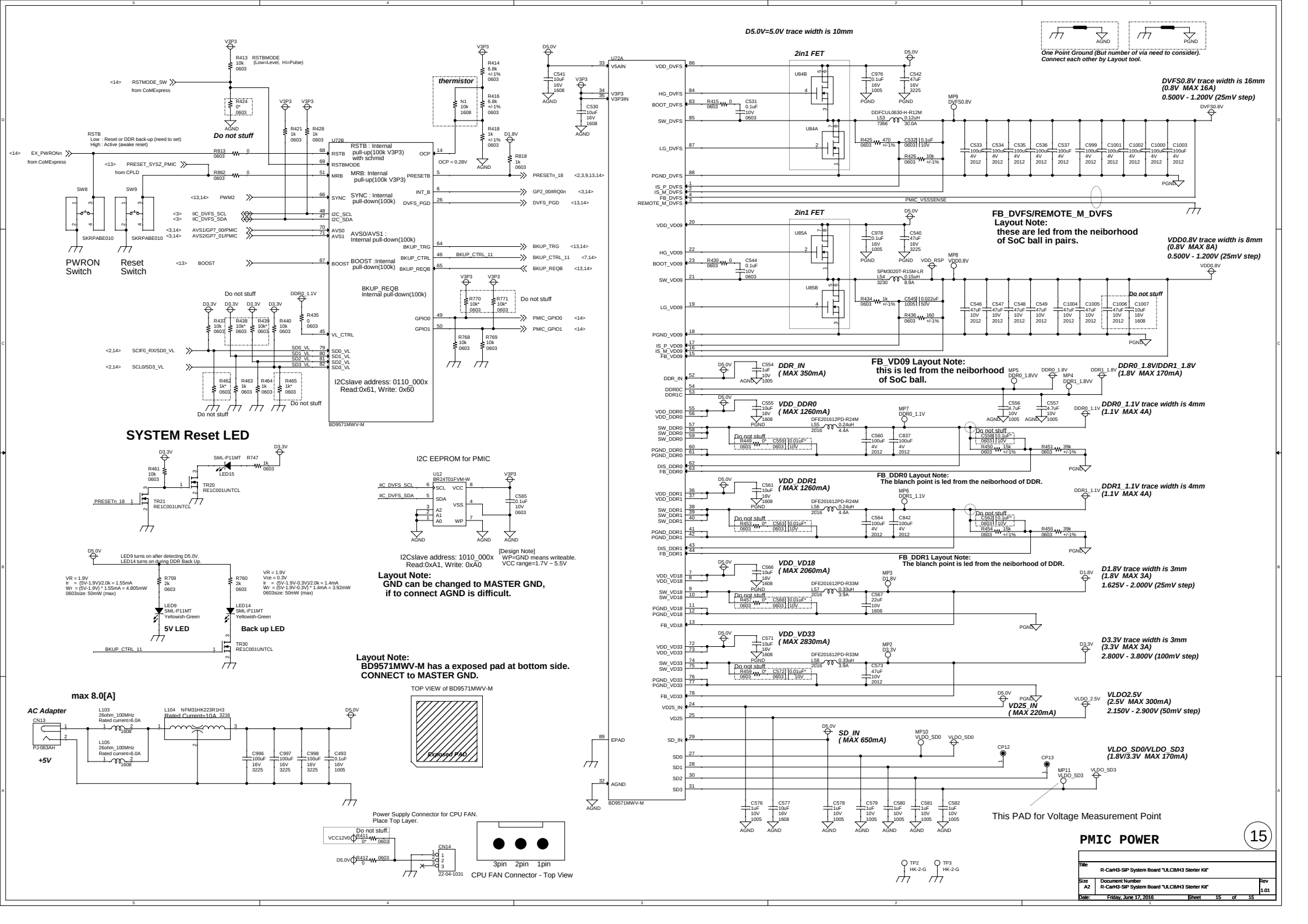
COM Express 440pin

VCC12V0
ULCB for CPU FAN.

R-CarH3 Module I/F

14

Title	R-CarH3-SiP System Board "ULCB/H3 Sterter Kit"		
Size A2	Document Number R-CarH3-SiP System Board "ULCB/H3 Sterter Kit"		Rev 1.01
Date: Friday, June 17, 2016	Sheet 14 of 15		


D5.0V=5.0V trace width is 10mm
One Point Ground (But number of via need to consider).
Connect each other by Layout tool.
AGND
PGND
2in1 FET
DVFS0.8V trace width is 16mm
(0.8V MAX 16A)
0.500V - 1.200V (25mV step)
FB_DVFS/REMOTE_M_DVFS
Layout Note:
these are led from the neiborhood
of SoC ball in pairs.
VDD0.8V trace width is 8mm
(0.8V MAX 8A)
0.500V - 1.200V (25mV step)
FB_VD09 Layout Note:
this is led from the neiborhood
of SoC ball.
DDR_IN
(MAX 350mA)
DDR0_1.8V/DDR1_1.8V
(1.8V MAX 170mA)
VDD_DDR0
(MAX 1260mA)
DDR0_1.1V trace width is 4mm
(1.1V MAX 4A)
FB_DDR0 Layout Note:
The blanch point is led from the neiborhood of DDR.
VDD_DDR1
(MAX 1260mA)
DDR1_1.1V trace width is 4mm
(1.1V MAX 4A)
FB_DDR1 Layout Note:
The blanch point is led from the neiborhood of DDR.
VDD_VD18
(MAX 2060mA)
D1.8V trace width is 3mm
(1.8V MAX 3A)
1.625V - 2.000V (25mV step)
VDD_VD33
(MAX 2830mA)
D3.3V trace width is 3mm
(3.3V MAX 3A)
2.800V - 3.800V (100mV step)
VD25_IN
(MAX 220mA)
VLDO2.5V
(2.5V MAX 300mA)
2.150V - 2.900V (50mV step)
SD_IN
(MAX 650mA)
VLDO_SD0/VLDO_SD3
(1.8V/3.3V MAX 170mA)
This PAD for Voltage Measurement Point
PMIC_VSSSENSE
PMIC POWER
SYSTEM Reset LED
I2C EEPROM for PMIC
I2Cslave address: 1010_000x
Read:0xA1, Write: 0xA0
[Design Note]
WP=GND means writeable.
VCC range=1.7V ~ 5.5V
Layout Note:
GND can be changed to MASTER GND,
if to connect AGND is difficult.
Layout Note:
BD9571MWV-M has a exposed pad at bottom side.
CONNECT to MASTER GND.
TOP VIEW of BD9571MWV-M
Exposed PAD
max 8.0[A]
AC Adapter
+5V
PJ-063AH
Power Supply Connector for CPU FAN.
Place Top Layer.
3pin 2pin 1pin
CPU FAN Connector - Top View
PWRON Switch
Reset Switch
Do not stuff
thermistor
I2Cslave address: 0110_000x
Read:0x61, Write: 0x60
BD9571MWV-M
R-CarH3-SiP System Board "ULCB/H3 Starter Kit"
Date: Friday, June 17, 2016
Sheet 15 of 15
15