

Initial Program Loader

Release Note: Software

R-Car H3/M3 Series

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Renesas Electronics

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How to Use This Manual

• [Readers]

This manual is intended for engineers who develop products which use the R-Car H3/M3 processor.

• [Purpose]

This manual is intended to give users an understanding of the functions of the R-Car H3/M3 processor device driver and to serve as a reference for developing hardware and software for systems that use this driver.

• [How to Read This Manual]

It is assumed that the readers of this manual have general knowledge in the fields of electrical

- engineering, logic circuits, microcontrollers, and Linux.
 - \rightarrow Read this manual in the order of the CONTENTS.
- To understand the functions of a multimedia processor for R-Car H3/M3
- \rightarrow See the R-Car H3/M3 User's Manual.
- To know the electrical specifications of the multimedia processor for R-Car H3/M3 \rightarrow See the R-Car H3/M3 Data Sheet.

• [Conventions]

The following symbols are used in this manual. Data significance: Higher digits on the left and lower digits on the right **Note**: Footnote for item marked with Note in the text **Caution**: Information requiring particular attention **Remark**: Supplementary information Numeric representation: Binary ... ××××, 0b××××, or ××××B Decimal ... ×××× Hexadecimal ... 0x×××× or ××××H Data type: Double word ... 64 bits Word ... 32 bits Half word ... 16 bits Byte ... 8 bits

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1. Introduction

1.1 Objectives

This manual explains the package construction of R-Car H3/M3 Initial Program Loader.

1.2 References

[1] Renesas Electronics Corp., Linux Interface Specification Yocto recipe Start-Up Guide.

[2] Renesas Electronics Corp., Initial Program Loader User's Manual.

This manual refers to the latest edition of the references.



2. Component

The following is included in this product.

2.1 Software components

The following shows components of ARM Trusted Firmware. Initial Program Loader is designed based on the architecture of BL2 and the part of BL1. BL31, BL32 are included R-Car H3/M3 Security Board Support Package. BL33 is Linux.

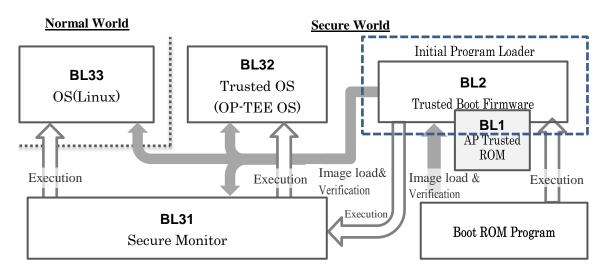


Figure 1 Software components

2.2 Software

Software is provided by the R-Car H3/M3 Yocto recipe.

Initial Program Loader is BL2 of ARM Trusted Firmware that is porting to R-Car H3/M3 platform. Initial Program Loader loads images and certificates of BL31, BL32, BL33, and verifies the images and certificates, and executes BL31.

The software is provided under a BSD 3-Clause license.

2.3 Initial Clock setting

Initial clock setting of each module at that time of exit for the Initial Program Loader is below.

2.3.1 R-Car H3 Ver.1.0

Module	Initial clock setting
Cortex-A57	1500 MHz
Cortex-A53	1200 MHz
3DGE	600 MHz
System (AXI-bus)	200 MHz
LPDDR4-SDRAM	DDR1600 (MD19=OFF/MD17=OFF)

2.3.2 R-Car H3 Ver.1.1

Module	Initial clock setting
Cortex-A57	1500 MHz
Cortex-A53	1200 MHz
3DGE	600 MHz
System (AXI-bus)	400 MHz
LPDDR4-SDRAM	DDR2400 (MD19=OFF/MD17=ON)



2.3.3 R-Car H3 Ver.2.0

Module	Initial clock setting
Cortex-A57	1500 MHz
Cortex-A53	1200 MHz
3DGE	600 MHz
System (AXI-bus)	400 MHz
LPDDR4-SDRAM	DDR3200 (MD19=ON/MD17=ON)

2.3.4 R-Car M3 Ver1.0 / Ver1.1

Module	Initial clock setting
Cortex-A57	$1500 \mathrm{~MHz}$
Cortex-A53	1200 MHz
3DGE	$600 \mathrm{~MHz}$
System (AXI-bus)	400 MHz
LPDDR4-SDRAM	DDR3200 (MD19=ON/MD17=ON)



3. Change History

Following change histories are representative lists.

3.1 v1.0.0

First release version.

3.2 v1.0.1

Fix and add about following restrictions and functions.

No.	Description
#77205	Version up the base version of arm-trusted-firmware.
	<u>https://github.com/ARM-software/arm-trusted-firmware</u> Commit e234ba038b0b997bd4325dad384deab5863babdd → 41099f4e7468d872857c52608dcc2a51bae68174
#79228	Updated QoS setting of arm-trusted-firmware.

3.3 v1.0.2

Fix and add about following restrictions and functions.

No.	Description
#79341	Remove the unused source code of DDR initialization.
#79391	Patch to separate DDR and QoS of source code.

3.4 v1.0.3

Fix and add about following restrictions and functions.

No.	Description
#80875	Corresponding GCC5.1 for poky2.0 GCC Compiler

3.5 v1.0.4

No.	Description
#83846	Add release process of STA restriction for H3 WS1.1.
#83584	Add clock setting process of SCIF2 for H3 WS1.1.
#83588	Add frequency set process of Generic Timer for H3 WS1.1.



3.6 v1.0.5

Fix and add about following restrictions and functions.

No.	Description
#77213	Add monitoring for IPL process hang-up. (Using system watchdog timer).
#79113	Update IPL boot message.
#81155	Add instruction cache disable/invalidate sequence.
#85275	Add display for verification failure message.
#85610	Add implementation for verification process of the BL33x Images.
#73723	Add initial voltage setting for PMIC.
#85121	Update the DDR/QoS settings for H3-WS1.1.

3.7 v1.0.6

Fix and add about following restrictions and functions.

No.	Description
#84155	Support Lossy Decompression using shared memory.
#84157	Delete size of version character.
#85127	Add setting to initialize RMSTPCR registers.
#77212	Add the address of Secure Boot API and LCS Judgment API for M3.
#72331	Add setting of pin functions for M3.
	Update the DDR settings for M3.
	Update the QoS settings for H3 WS1.0/M3.
	Add the DDR software version for M3.
#87678	Delete setting of SYS-DMAC2 by IPL.
#87765	Add initializing process of IPMMU registers.
#89216	Update the DDR settings rev.0.15 for H3 WS1.1.

3.8 v1.0.7

No.	Description
#80050	Change the order of the CPG initialization.
#80496	Change the order of the QoS initialization.
#88794	Add SCIF2 resource release.
#86876	Modify some inline function to function.
#88259	Change the make argument default value of RCAR_SECURE_BOOT.
#90373	Update the DDR settings for M3.
#89944	Add workaround for PFC write access problem, to PFC initialization.
#90658	Update the QoS settings for M3.
#90662	Add workaround by RT-DMAC, for PFC write access problem.



3.9 v1.0.8

Fix and add about following restrictions and functions.

No.	Description			
#92129	Add compile switch for Lossy.			
	"RCAR_LOSSY_ENABLE"			
	If this option value is 0, Lossy Decompression is disable. If this option value is 1, it is enable.			
#92045	Add setting of register CA53DBGRCR.			
#86598	Iodify the problem BL31 built with DEBUG=1 does not start.			
#88873	Modify build error that occurred when using LOGLEVEL=0 or 10.			
#79402	Add settings SECURITY protection, SDRAM protection, SRAM protection.			
#90662	Modify workaround by RT-DMAC, for PFC write access problem.			
#92752	Update the QoS settings for M3.			
#91784	Modify code to become compatible Binary in case of CA57/53 boot and CR7 boot.			

3.10 v1.0.9

Fix and add about following restrictions and functions.

No.	Description			
#97222	[H/W Restriction No.58] Change the CA5xBAR address from SystemRAM to SDRAM.			
	(The execution module of this process is changed from Initial Program Loader to Secure			
	Monitor)			
#98480	Add the compile option of LIFEC_DBSC_PROTECT_ENABLE.			
#97932	[H/W Restriction No.38] Fix the AXI-bus errata.(Wait 10us after the LifeC settings)			
#87840	Change the load destination address of the LOADER to the 64-bit address region.			
#97962	Fix the issue do not restart by software reset by SystemWDT.			
#86030	Add the report message to exception handling.			
#99015	Change a path of #include header file to not use a related path.			
#86022	Add the feature of Suspend to RAM.			
#86509	Add the eMMC boot.			
#97865	[H/W Restriction No.23] Update the QoS settings.			

3.11 v1.0.9.10

No.	Description	
#100382	Clean-up to the DDR setting code.	



3.12 v1.0.10

This version branched from v1.0.9.

Fix and add about following restrictions and functions.

No.	Description	
#103604	Change u-boot boot address to 0x50000000 from 0x49000000.	

3.13 v1.0.11

Fix and add about following restrictions and functions.

No.	Description	
#107771	Integrate v1.0.9.10 and v1.0.10 into v1.0.11.	

3.14 v1.0.12

No.	Description			
#99411	Update H3 WS1.0/WS1.1 QoS setting rev.0.33.			
	Update M3 WS1.0 QoS setting rev.0.16.			
#99473	Add binary compatible build option with H3 and M3.			
#101134	hange conditions for applying security settings. (CR7 boot was excluded)			
#103077	Organizing constants for the certificate header (SA6) of the dummy tools.			
#104125	H/W Restriction No.65] Fix workaround by RT-DMAC, for PFC write access problem.			
#105357	Support 40bit address for Lossy area.			
#105866	Fix build error in DEBUG case.			
#108783	Version up the base version of arm-trusted-firmware.			
	https://github.com/ARM-software/arm-trusted-firmware			
	Commit ID 6bb37adc203567c2f9322dfbe34058a5f12d4c70 [Tag: v1.3]			
#108711	Update the DRVCTRL register setting.			
#108757	Fix algorithm for loading multiple non-secure target program images.			
#109215	Fix protection range settings for the System RAM. (0xE6320000 -> 0xE6302000).			
#110057	Add build option to select the OP-TEE loading.			
#110100	10100 Change the message. It calls attention to the user when hanging with DipSW setting mismatch (especially assuming SW 7 - pin 1),			



3.15 v1.0.13

No.	Description				
#110616	Fix the pointer arithmetic of Lossy code that pointed out by static code analysis tool.				
#114766	orrespond to new memory map.				
#112792	ix the parameter of authentication API for H3 Ver2.0.				
#114333	Change to obtain lifecycle state from library function.				
#112785	Change display format of the product version.				
#113054	[H/W Restriction No.82] Clear SError in bl2 entrypoint.				
#112484	dd the PFC setting for H3 Ver2.0.				
#114296	Add MFIS register setting.				
#112483	Update DDR setting for H3 Ver2.0.				
#112482	Add the QoS setting for H3 Ver2.0, update H3 Ver1.1, Ver1.0, M3.				
#115944	BL2: reset: Enable generic counter and enable BL2 timestamps.				
#116824	plat: rcar: Initialize console only for CA5x boot.				
#117769	plat: renesas: rcar: Change of the board judgement.				
#117895	Update DDR setting rev.0.22.				
#117377	Update H3 v20 QoS setting rev.0.12.				
#117298	Add distinction to board and change the setting of GenericCounter.				
#115929	Change definition name of the PLL multiplication ratio setting (MD14, MD13).				
#116084	Change Add build option for disable the PMIC related function.				
#116706	Add check loading area for BL33 to BL338.				
#117296	Fix SRAM protection range.				
#117326	Fix if BL32 loading fails, stop BL2.				



3.16 v1.0.14

Fix and add about following restrictions and functions.

No.	Description	
#102234	Fixed the high-speed mode setting sequence for the eMMC.	
#106706	Correspond to the eMMC boot using same boot partition as the Boot ROM.	
#117377	Add the QoS setting for M3 Ver1.1, update H3 Ver1.1, H3 Ver2.0.	
#117709	Add Board name to serial log output.	
#118918	plat: renesas: rcar: Add power off for Starter Kit.	
	plat: renesas: rcar: Add ULCB CPLD support.	
#102355	Fix the comments in source codes.	
#107378	Correspond to make the SDHI (DMAC) specification change.	
#109690	QAC pointed out correspondence.	
#114878	Fix flush process of the Console FIFO.	
#119078	Modify the System/Secure Module Stop Control Settings.	
#119178	plat: io_rcar: Fix typos.	
#119394	Ensure unique timestamps for multiple tf_printf0 calls.	
#119576	Modify version display of the M3 Ver2.0 to "M3 Ver1.1".	
#119873	Update the QoS setting for H3 Ver2.0, M3 Ver1.1.	
#120782	Delete debug code.	
#120834	BL33x loadable range check does not work properly.	

3.17 v1.0.15

No.	Description			
#122536	H/W Restriction No.71 #9] BL2: Disable TLB cache function of IPMMU caches.			
#122541	pdate the QoS setting for H3 Ver1.0/1.1/2.0, M3 Ver1.0/1.1.			
#123541	Update DDR setting (rev0.23).			
#123206	plat: rcar: ddr: Add missing PMIC_ON_BOARD macro.			
#123212	at: rcar: io storage: drv_policies is rw.			
#123374	Change Timeout of eMMC.			
#124005	Modify conflict by the IIC for DVFS processing.			
#124730	Update H3 Ver1.0 QoS setting rev.0.36.			
	Update H3 Ver1.1 QoS setting rev.0.37.			
	Update H3 Ver2.0 QoS setting rev.0.16.			
	Update M3 Ver1.0 QoS setting rev.0.19.			
	Update M3 Ver1.1 QoS setting rev.0.13.			
#126475	Changed code comment on time measurement function using the TMU ch3.			
#126911	Update DDR setting (rev0.24).			
#127015	Change initial voltage setting for PMIC.			

3.18 v1.0.16

No.	Description			
#126556	Change CPG setting.			
#128036	Update H3 Ver2.0 QoS setting rev.0.17.			
	Update M3 Ver1.1 QoS setting rev.0.14.			
#128037	Update DDR setting (rev0.25).			
#128054	Fix typos (comments of execDMA).			
#128344	Replace PMIC_ON_BOARD macro with some new macros that correspond to the function.			
#128539	Changed the specification of the initial voltage setting for PMIC.			
#130052	Modify the variable names and comments in dummy_create.			
#130980	Add the board name for serial log output.			
#132663	Update H3 Ver2.0 QoS setting rev.0.18.			
	Update M3 Ver1.1 QoS setting rev.0.16.			
#132664	Update DDR setting (rev0.27).			
#133221	Modify return and unnecessary definition of scif.			
#133355	Change the ARMREG register setting.			



4. Confirming the execution software components

When you confirm executing Initial Program Loader, please follow the documents [1] . The hardware environment is below.

```
· SoC
```

- R-Car H3/M3
- $\cdot \ \text{Board}$
 - System Evaluation Board "Salvator-X" System Evaluation Board "Salvator-XS"



5. Restrictions

There is no restriction in this revision.



Initial Program Loader Release Note: Software

Rev.	Date		Description
		Page	Summary
1.0.0	Sep. 30, 2015		New creation.
1.0.1	Nov. 23, 2015	1	 1.2 References Updated Linux Interface Specification Yocto recipe Start-Up Guide has updated. 3.Changes between previous revision
		3	Updated changes between previous revision.
1.0.2	Dec. 07, 2015	3	3.Change History (rename from "3.Change between previous revision") 3.3 add history of v1.0.2.
1.0.3	Feb. 12, 2016	3	3.Change History 3.4 add history of v1.0.3.
1.0.4	Feb. 23, 2016	3	3.Change History 3.5 add history of v1.0.4.
	Mar. 25, 2016	2	2.Component 2.3. Initial clock setting Added the Initial clock setting information.
1.0.5		4	3.Change History 3.6 add history of v1.0.5.
		6	5.Restrictions Updated the description of the contents are not supported in this revision.
	Apr. 27, 2016	1	 1.1 Objectives Added platform 'M3'. 1.2 References Updated Linux Interface Specification Yocto recipe Start-Up Guide has updated. Add Initial Program Loader User's Manual.
1.0.6		2	2.1 Software components 2.2 Software Added platform 'M3'.
		3	2.3. Initial clock setting Added the Initial clock setting information of R-Car M3.
		5	3.Change History 3.7 add history of v1.0.6.
		6	4.Confirming the execution software components Add platform 'M3'.
		7	5.Restrictions Added restriction about DRAM split setting and option of LOG_LEVEL.
	May 27, 2016	1	1.2 References Add description about revision of the references.
1.0.7		3	2.3. Initial clock setting Changed LPDDR4-SDRAM information of R-Car M3.
		5	3.Change History 3.8 add history of v1.0.7.
		7	5.Restrictions Deleted restriction about DRAM split setting.
1.0.8	lup 20 2016	6	3.Change History 3.8 add history of v1.0.8.
1.0.0	Jun. 30, 2016	8	5.Restrictions Removed a restriction in this revision (4).
1.0.9	Aug. 29, 2016	6	3.Change History 3.9 add history of v1.0.9.
		8	5.Restrictions Removed a restriction in this revision.
1.0.9.10	Nov. 2, 2016	6	3.Change History 3.10 add history of v1.0.9.10.
1.0.10	Oct. 26, 2016	7	3.Change History

			3.11 add history of v1.0.10.
1.0.11	Nov. 22, 2016	7	3.Change History 3.12 add history of v1.0.11.
1.0.12	Dec. 22, 2016	7	3.Change History 3.13 add history of v1.0.12.
1.0.13	Mar. 15, 2017	2,3	2.3 Initial Clock setting Changed "R-Car H3 WS" to "R-Car H3 Ver." Added the Initial clock setting information of R-Car H3 Ver.2.0.
		8	3.Change History 3.13 add history of v1.0.13.
1.0.14	Apr. 10, 2017	2,3	2.3 Initial Clock setting Changed to 2.3.4 R-Car M3 Ver.1.0 / Ver1.1 from 2.3.4 R-Car M3.
		9	3.Change History 3.16 add history of v1.0.14.
		10	4. Confirming the execution software components Added the "Salvator-XS" board.
1.0.15	Jun. 14, 2017	9	3.Change History 3.17 add history of v1.0.15.
1.0.16	Aug. 24, 2017		Fixed the format of the document (trademark, etc.)
		10	3.Change History 3.18 add history of v1.0.16.

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Initial Program Loader Release Note

