R-CarD3 System Evaluation Board "Draak"

RTP0RC77995SEB0010S

Rev0.29

Preliminary

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Size: A2	Document Number: R-CarD3 System Evaluation Board(Draak)	Rev: 0.29
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Layout Note:
Following signals need Ground guard.

AUDIO_CLKA
SCIF_SCK1/AUDIO_CLKOUT1/GP4_22
AUDIO_CLKOUT/SSI_SCK4

CAN_CLK/IRQ5/GP5_02_D3 until X13-pin3

MMC0_CLK,eMMC_CLK_18

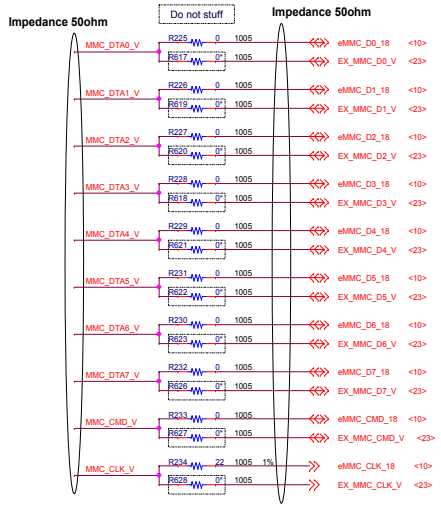
AVB0_TXCREFCLK_VL
AVB0_TXC_VL
AVB0_RXC_VL

QSPI0_SPCLK_18
QSPI1_SPCLK_18

Layout Note:
As short as possible from U1(D3) to two Rxxx.

Two Rxx SpecialPAD

Want level



Layout Note:
Following signals need Ground guard.

MMC_CLK_V,eMMC_CLK_18,EX_MMC_CLK_V

CAN Clock

R-CarD3_DU/VI4

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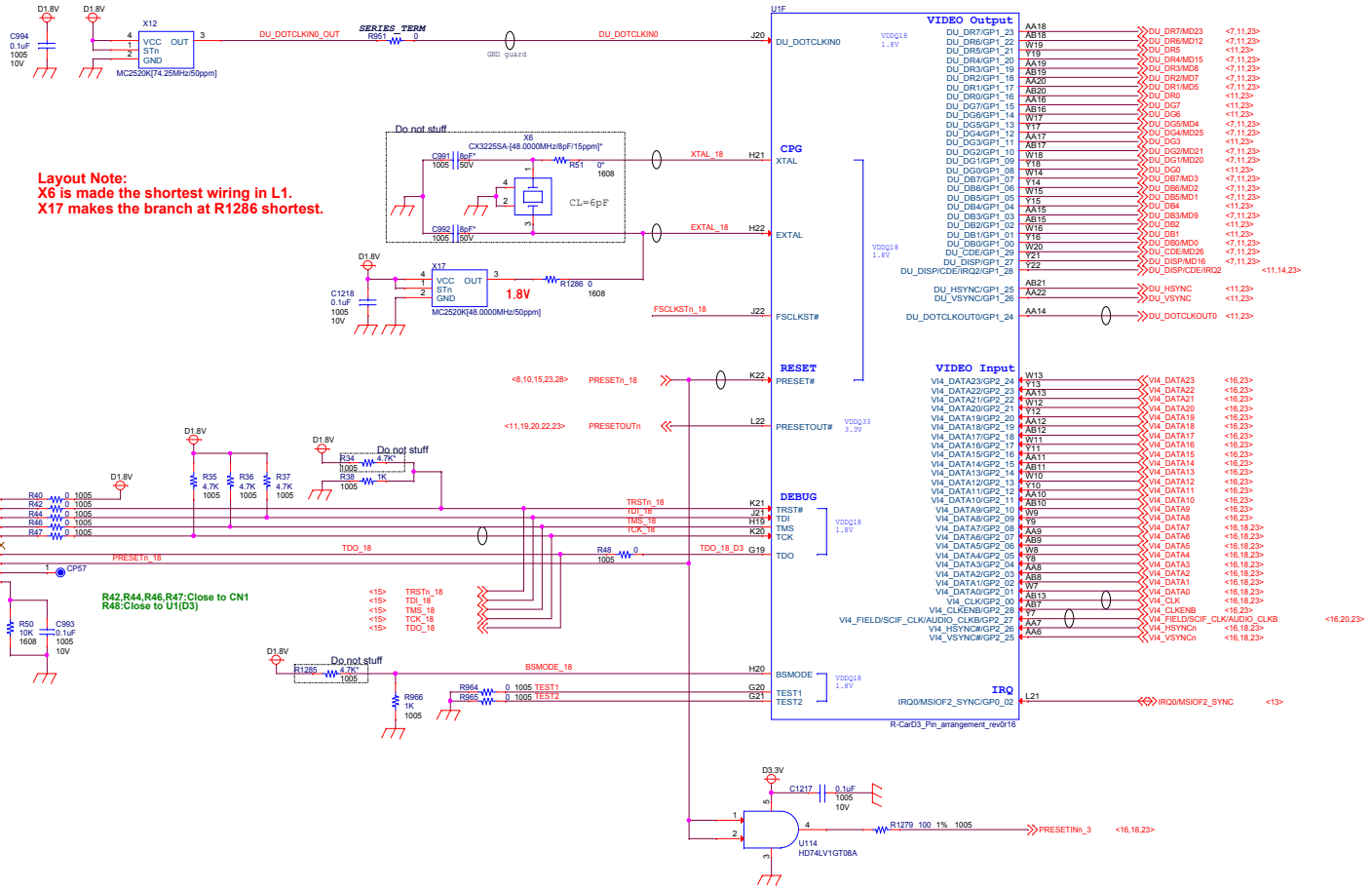
Layout Note:
Following signals need Ground guard.

DU_DOTCLKIN0 until X12 3pin
DU_DOTCLKOUT0
VI4_CLK

XTAL_18,EXTAL_18
PRESETn_18
TCK_18



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R-CarD3_USB/LVDS

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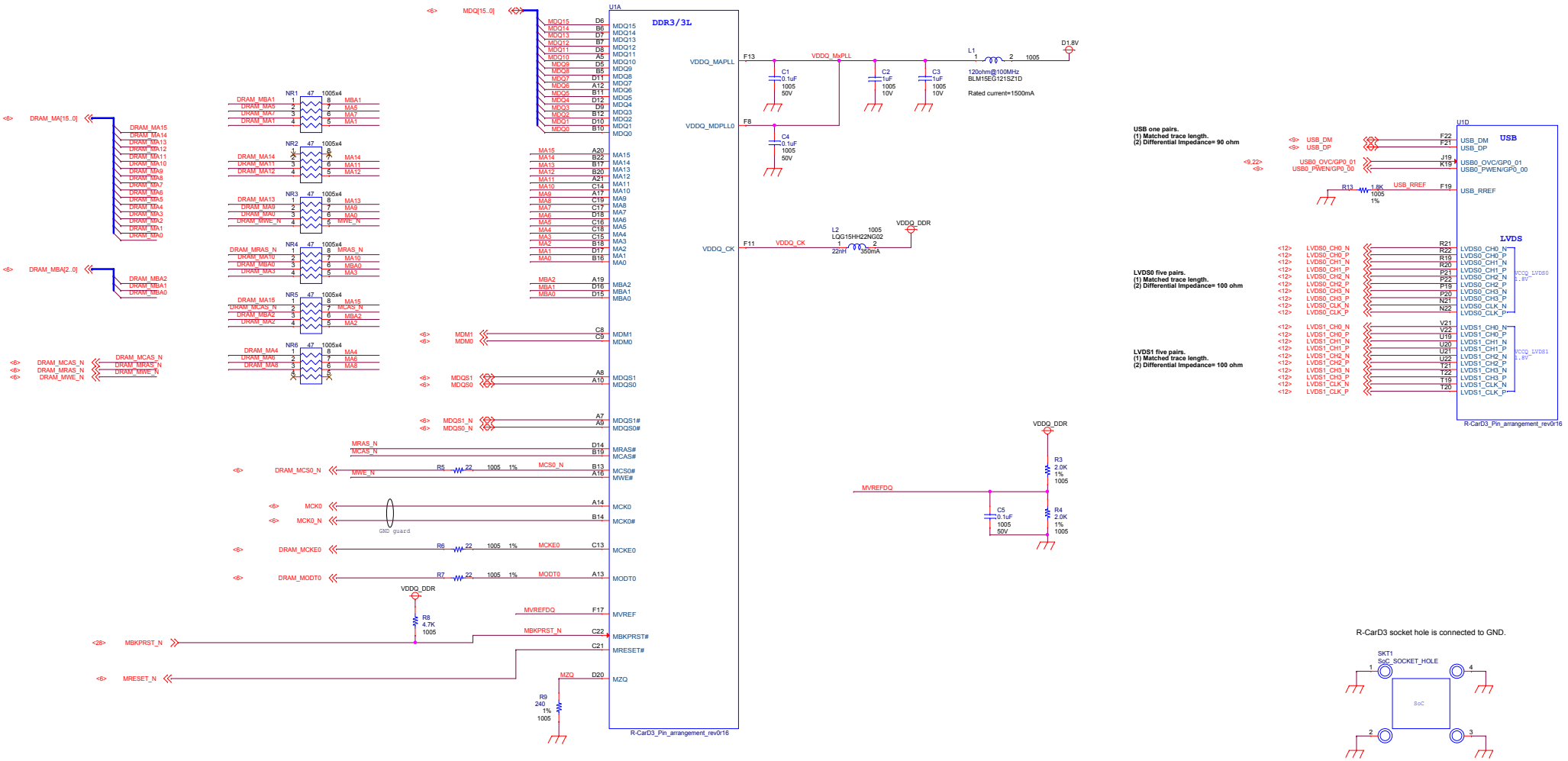
Layout Note:
Following signals need Ground guard.

MCK0,MCK0_N



R-CarD3 socket hole is connected to GND.

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R-CarD3_DDR3

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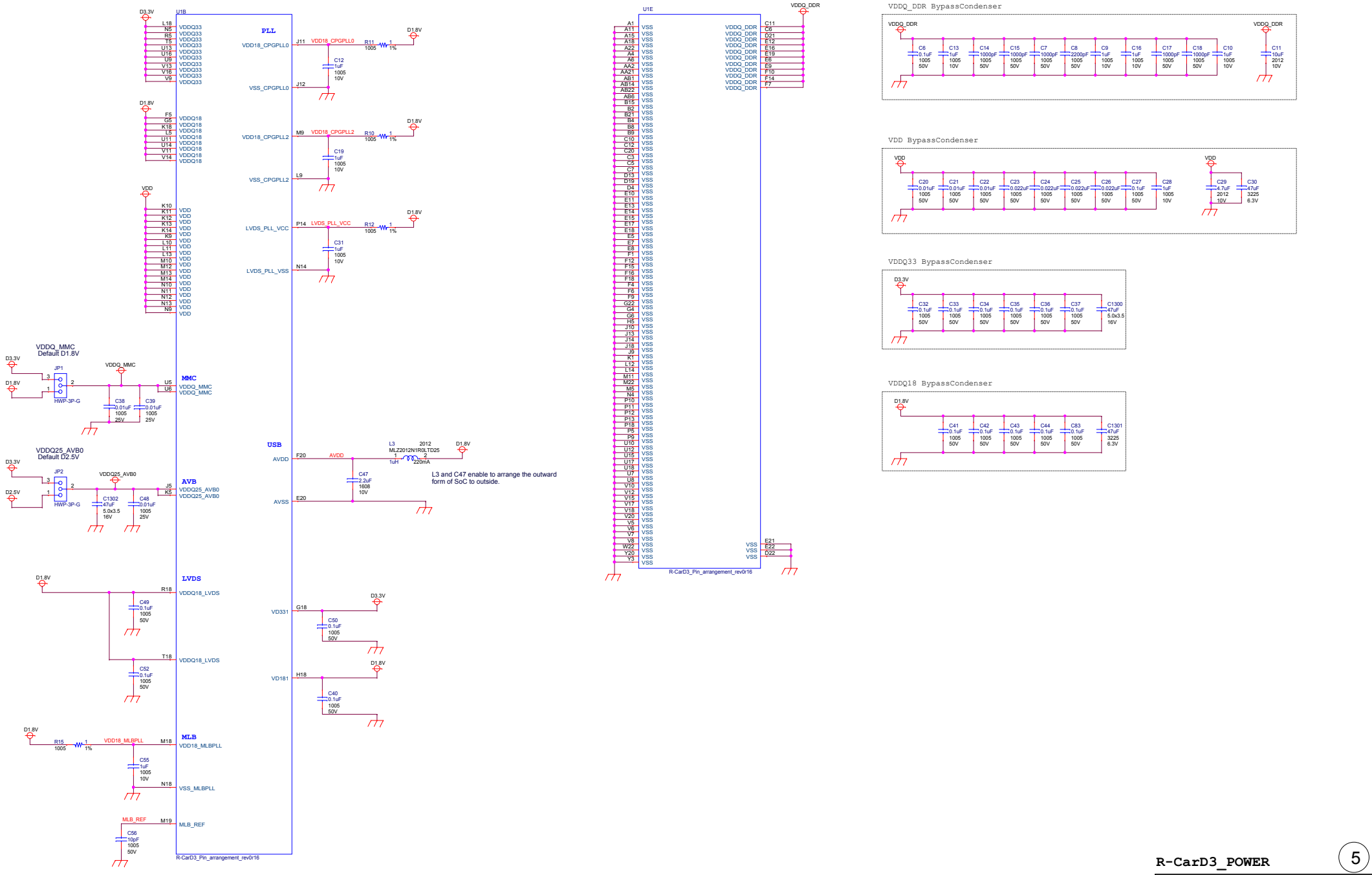

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R-CarD3_POWER

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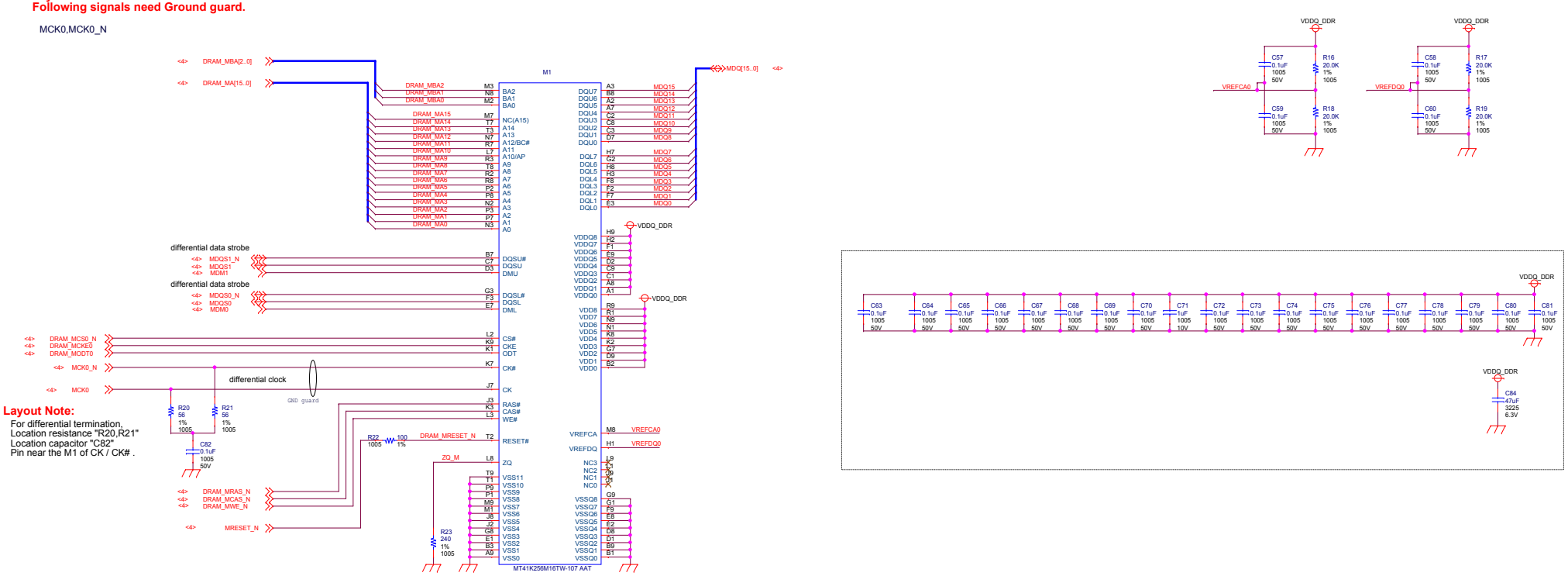

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DDR3_SDRAM

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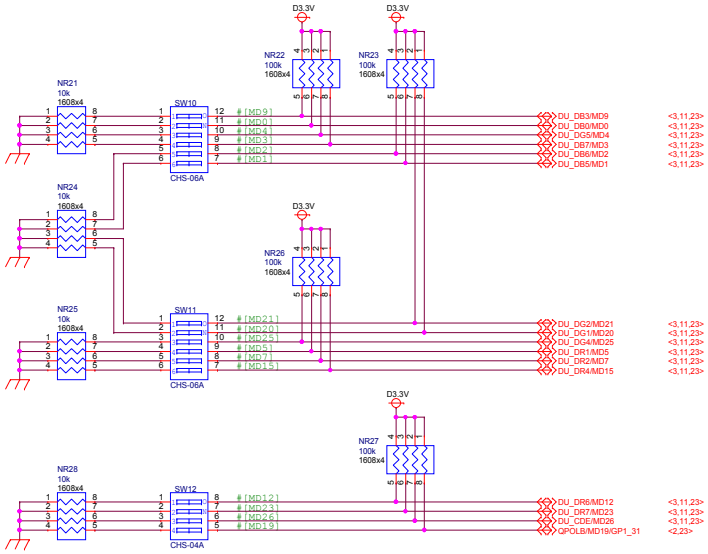
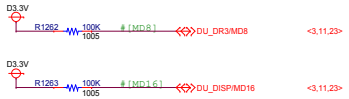
Layout Note:
Mode switches must be placed on Top Layer.

Layout Note:
MD* Line reduce a stub as much as possible.

MODE SW





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MODE_SW

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Layout Note:
(1)As short as possible from D3 to Hyper Flash.
(2)Branches from the nearby Hyper Flash side to the SW1,SW2.
As short as possible from D3 to SW1, SW2.

Layout Note:
As short as possible from D3 to Hyper Flash.
(Assume that it's taken top priority over other wiring.)

Hyper FLASH / Octal FLASH (512Mbit)

U110 S26KS512SDPBHV02

< U86 Table >	R941,R943,R944, R945,R946	R942	R948
S26KS512SDGBHV02	Mount	Mount	Mount
MT35XQLKAU512ABA	No Mount	Mount	No Mount
MX25UM51245G	No Mount	Mount	No Mount

[Design Note]
SW42,R949,R950=Used in mt35xqlkaU512ABA

Layout Note:
-QSPI0_MOSI_IO0_18,QSPI0_MISO_IO1_18,QSPI0_IO2_18,QSPI0_IO3_18,QSPI1_MOSI_IO0_18, QSPI1_MISO_IO1_18,QSPI1_IO2_18,QSPI1_IO3_18(=DQ[0:7] line) and QSPI1_SSL_18-RDS_FLASH_18 should have the same number of vias and layer changes. (recommended to route the DQ[0:7] line and QSPI1_SSL_18-RDS_FLASH_18 on the same signal layer.)

-QSPI0_SPCLK_18 and QSPI1_SPCLK_18 should be routed in a coplanar fashion while maintaining single ended impedance of 50 ohms and differential impedance of 100 ohms (nominal value).

When using the Hyper Flash, wiring as possible so as not to short stub.

SPI FLASH (128Mbit/QSPI0)

SW 1-2 short : Internal SPI FLASH Effective
SW 2-3 short : External SPI FLASH Effective

U5 S25FS128SAGMFV10

-Length matching recommendations

Signal Group	Length Match Tolerance
QSPI0_SPCLK_18 to QSPI1_SPCLK_18	+/- 10mils
QSPI1_SSL_18-RDS_FLASH_18 to DQ[0:7] line	+/- 25mils
DQx(0-7) line to DQy(0-7) line	+/- 50mils
QSPI0_SPCLK_18/QSPI1_SPCLK_18 to DQ0-7 line	+/- 500mils
QSPI0_SPCLK_18/QSPI1_SPCLK_18 to QSPI0_SSL_18 - CSn_FLASH_18	+/- 1500mils
QSPI0_SPCLK_18/QSPI1_SPCLK_18 to QSPI1_SSL_18-RDS_FLASH_18	+/- 1500mils
RPC_RESETn_18 to QSPI0_SSL_18 - CSn_FLASH_18	+/- 2000mils

It is recommended to keep the RPC_RESETn_18 trace short.

-Additionally refer to "HyperBus memory PCB Design Recommendation"

EX-SPI Connector (QSPI0)

PSM-410336-09
SMT PinHeader

EX-SPI Connector (QSPI1)

PSM-410336-09
SMT PinHeader

Layout Note:
From SW to PinHeader will be wiring so that it is not visible to the stub becomes a branch.

SW : SW1, SW2
PinHeader : CN3, CN4

EX-SPI-Flash-Board generate VIO=1.8V from D3.3V for internal using.

I2C EEPROM

U57 BR24T01FVM-W

I2Cslave address: 1010_000x [Design Note]
Read:0xA1, Write: 0xA0 WP=GND means writeable.
VCC range=1.7V ~ 5.5V

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QSPI_FLASH/Hyper_FLASH 8

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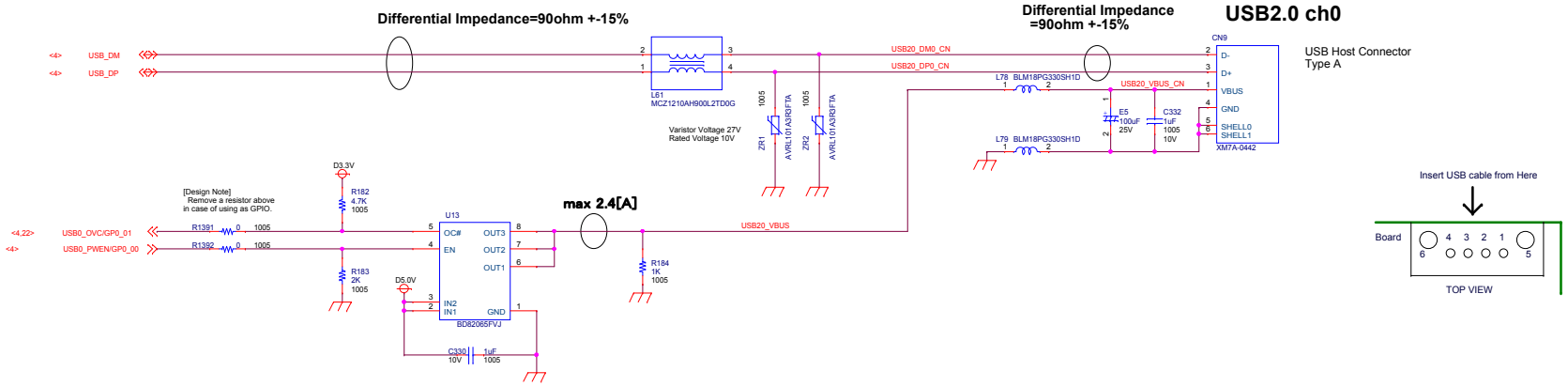
Layout Note:
As short as possible from CN9 to L61, ZR1 and ZR2.
Reduce Stub.



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USB2.0

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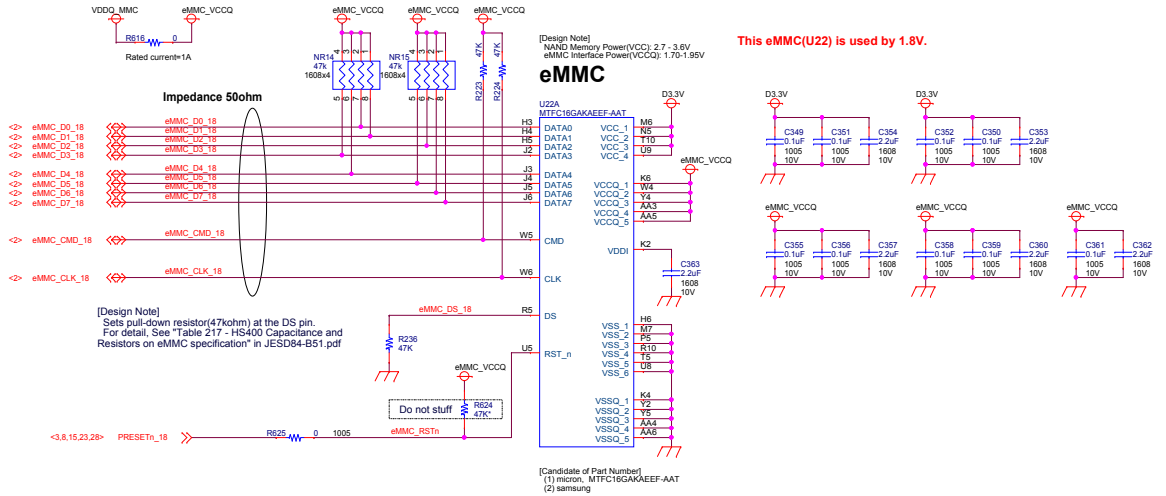

[Design Note]
In case of using NAND through EXIO connector "EXIO_B",

DISMOUNT follwoing resistors.
R229, R231, R230, R232(0ohm/1005).
and MOUNT following resistors.
R621, R622, R623, R626(0ohm/1005).

DISMOUNT follwoing resistors
R225, R226, R227, R228, R233, R234(0ohm/1005)
R625(0ohm/1005) for PRESETn_18
and MOUNT following resistors.
R617, R619, R620, R618, R627, R628(0ohm/1005)

and MOUNT following resistors.
R224(47k/1608) to prevent eMMC's CLK-pin floating.
R624(47k/1608) to prevent eMMC's RST_n-pin floating.

Layout Note:
Following signals need Ground guard.

eMMC_CLK_18

Layout Note:
Matched Trace Length from R-CarD3 to eMMC. max 200Mbps/pin

Group 1
MMC_DTA[7:0]_V + eMMC_D[7:0]_18
MMC_CMD_V + eMMC_CMD_18
MMC_CLK_V + eMMC_CLK_18

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MMC0

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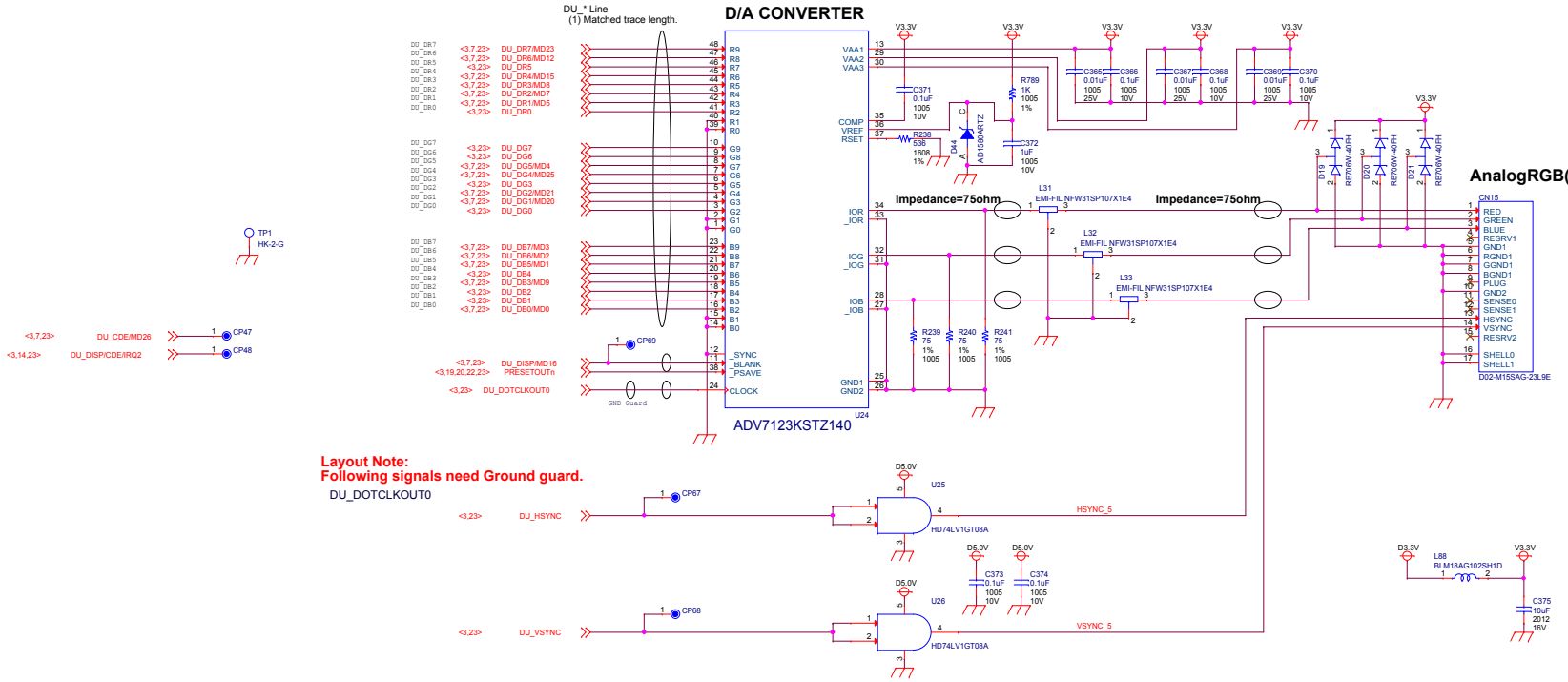

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DU_ARGB

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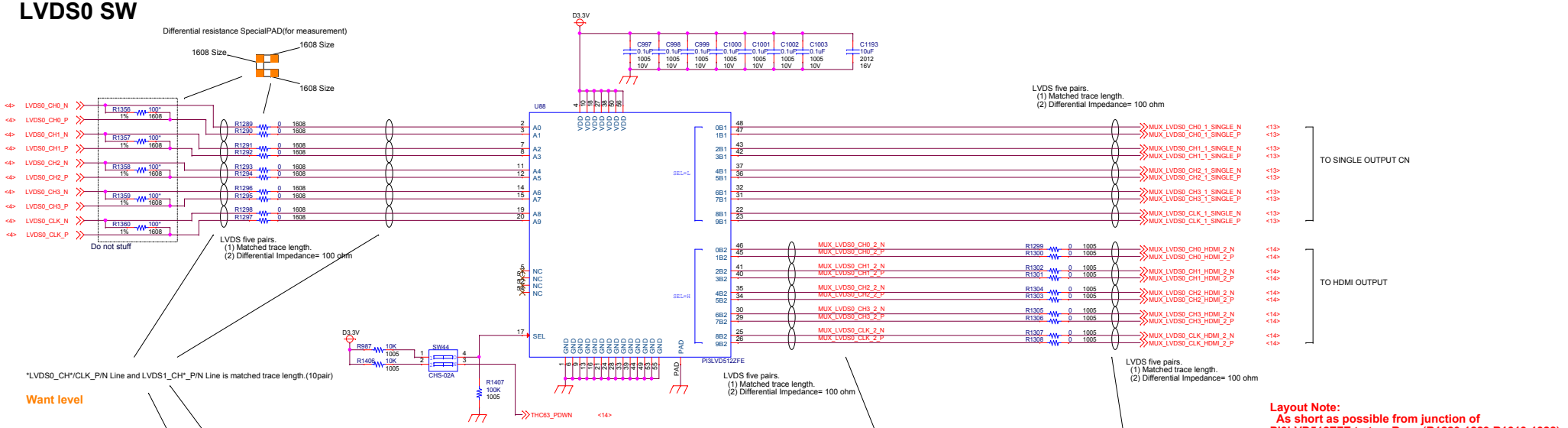
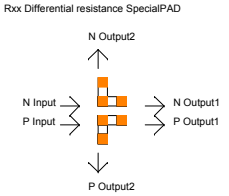
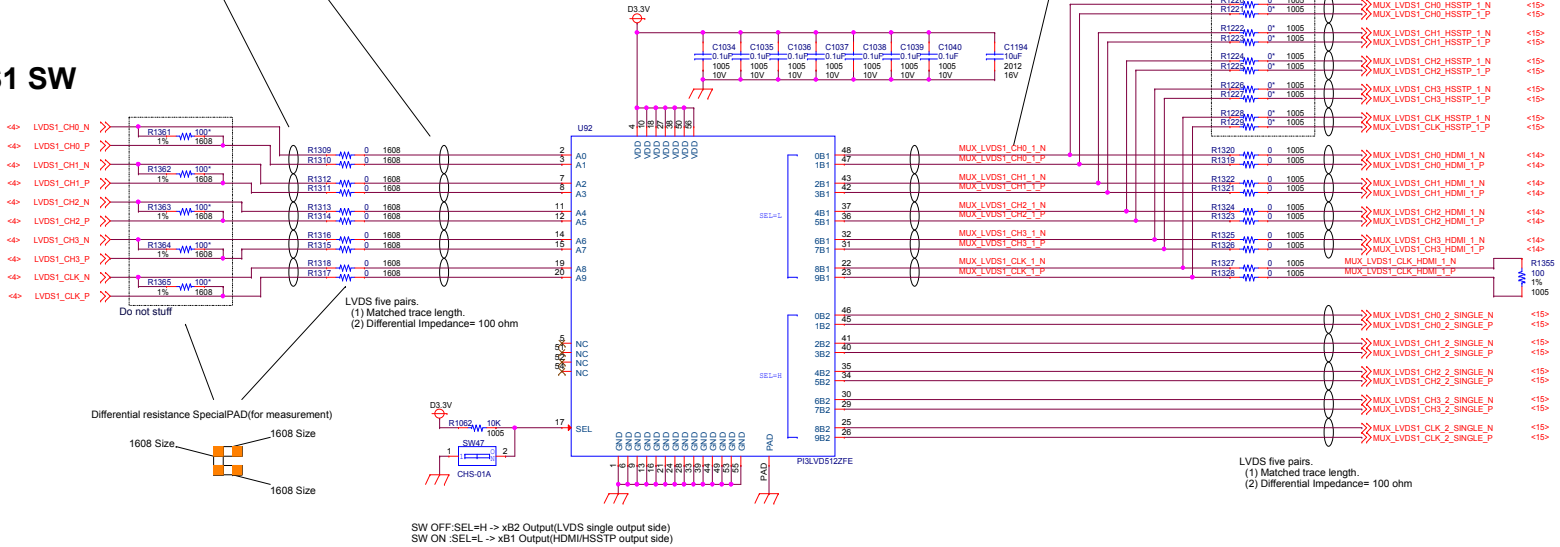
LVDS0 SW



Layout Note:
As short as possible from junction of PI3LVD512ZFE to two Rxxx.(R1220-1229,R1319-1328)



LVDS1 SW



LVDS (OUTPUT SW)

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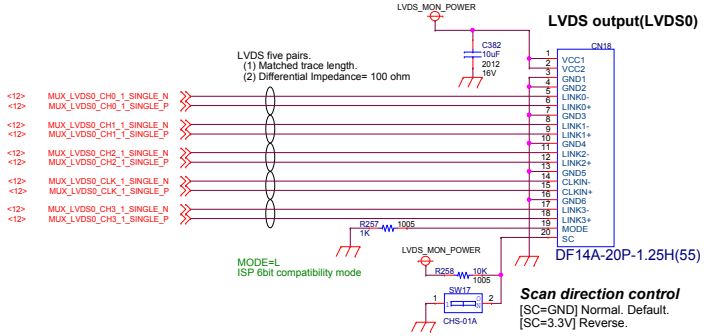
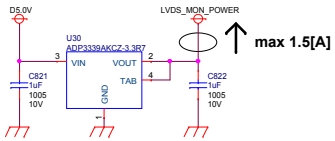
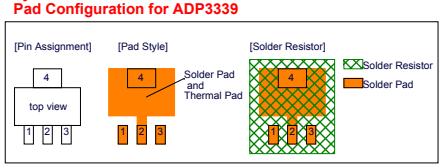


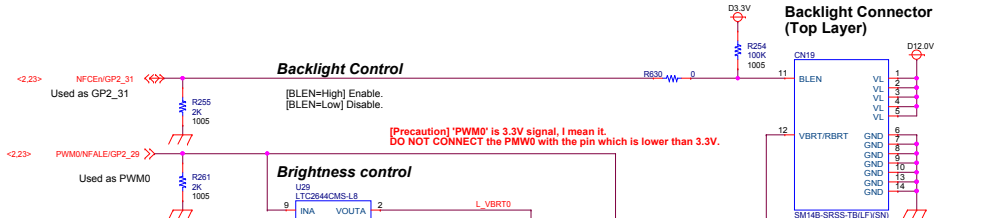
3.3V for LVDS Monitor Power



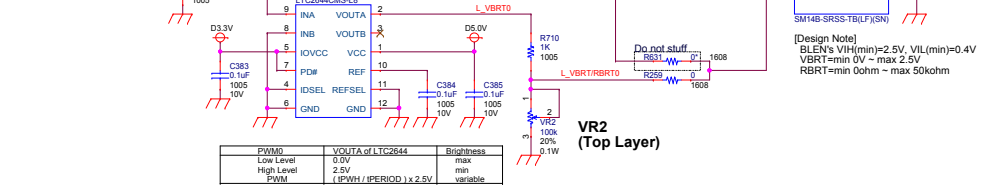
Layout Note: Pad Configuration for ADP3339



Backlight Control



Brightness control



VR2 (Top Layer)

Backlight Connector (Top Layer)

[Design Note]
BLEN's VIH(min)=2.5V, VIL(min)=0.4V
VBRT=min 0V ~ max 2.5V
RBRT=min 0ohm ~ max 50kohm

PWM0	VOUTA of LTC2644	Brightness
Low Level	0.0V	max
High Level	2.5V	min
PWM	(tPWH / tPERIOD) x 2.5V	variable

[Design Note]
LTC2644HMS-L8#TRPBF for Automotive.

LVDS CONT CONNECTOR

LVDS0(SINGLE OUT)

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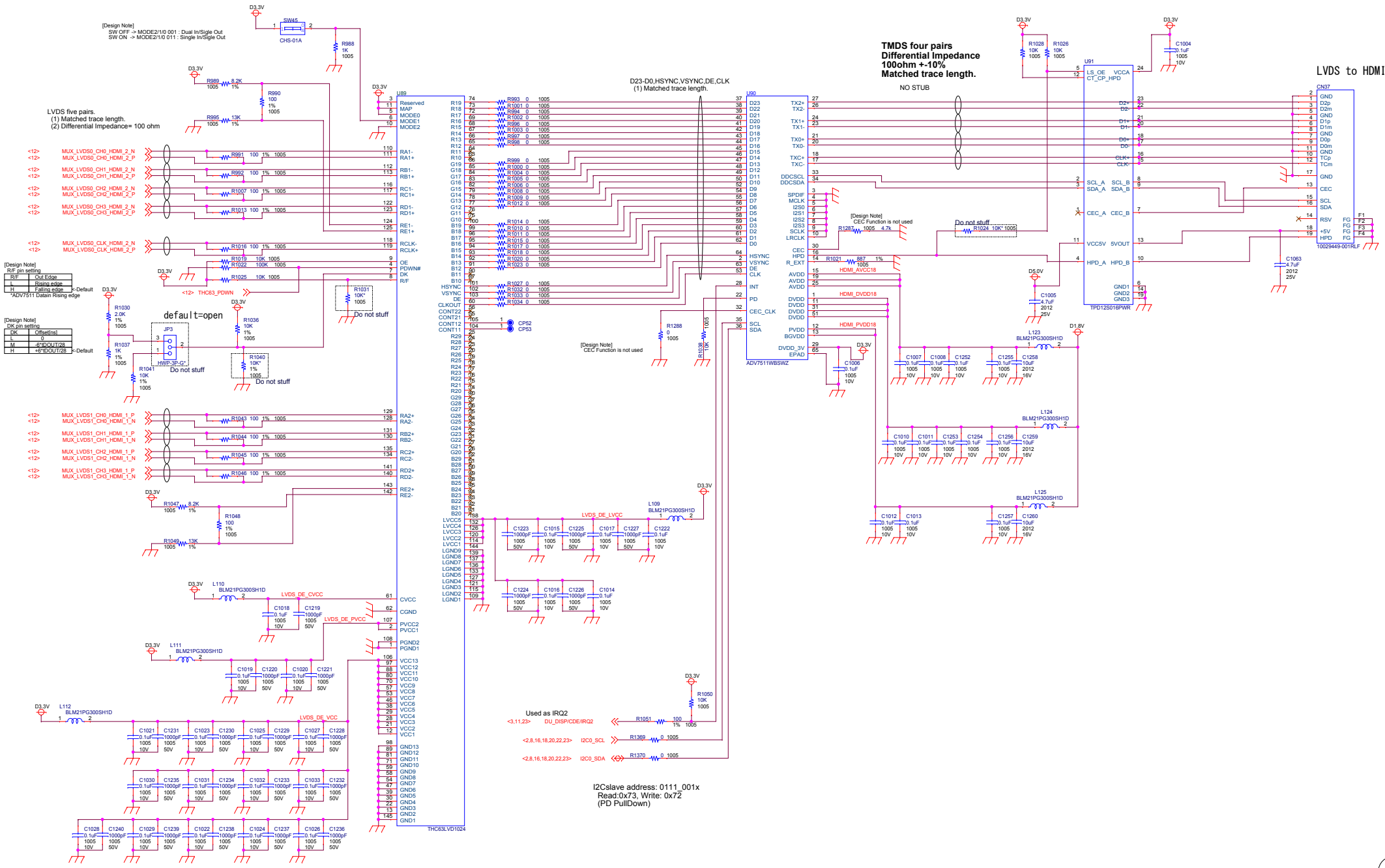

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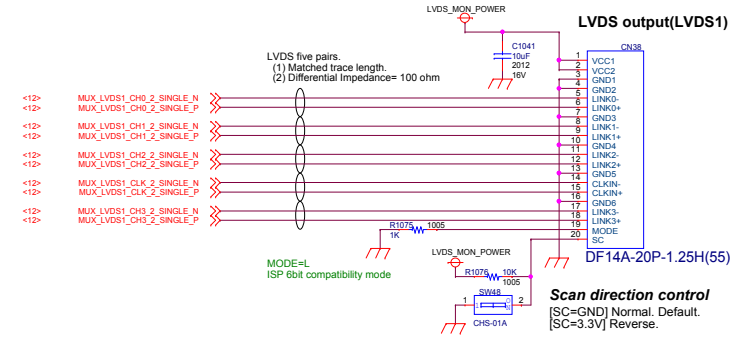
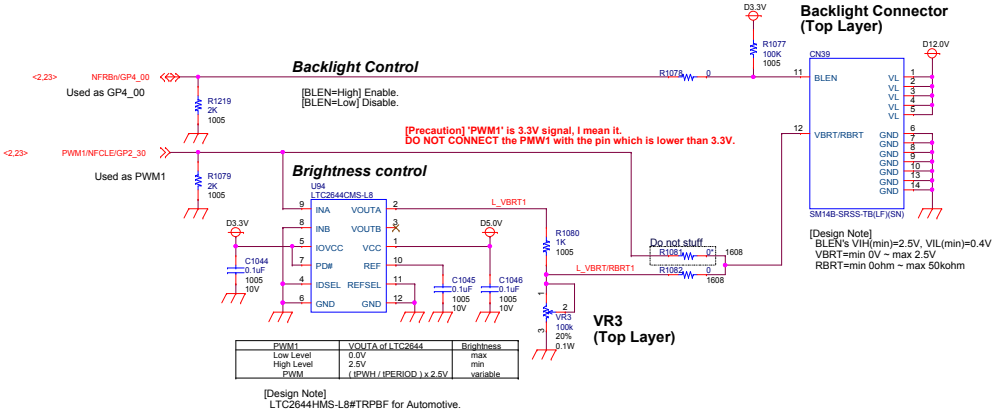
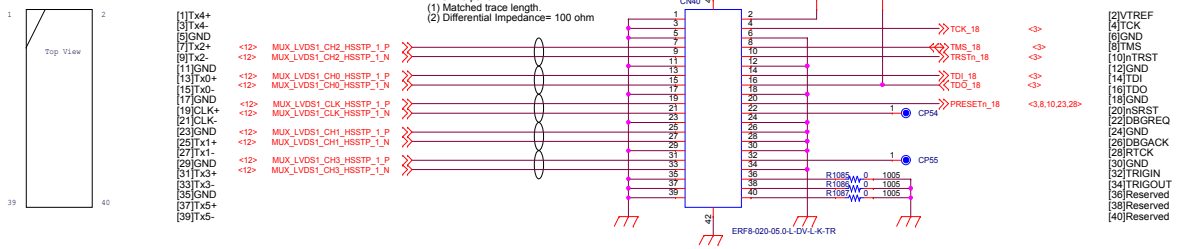




#[HSSTP 40pin]

HSSTP Connector(LVDS1 OUT)
(Top Layer)



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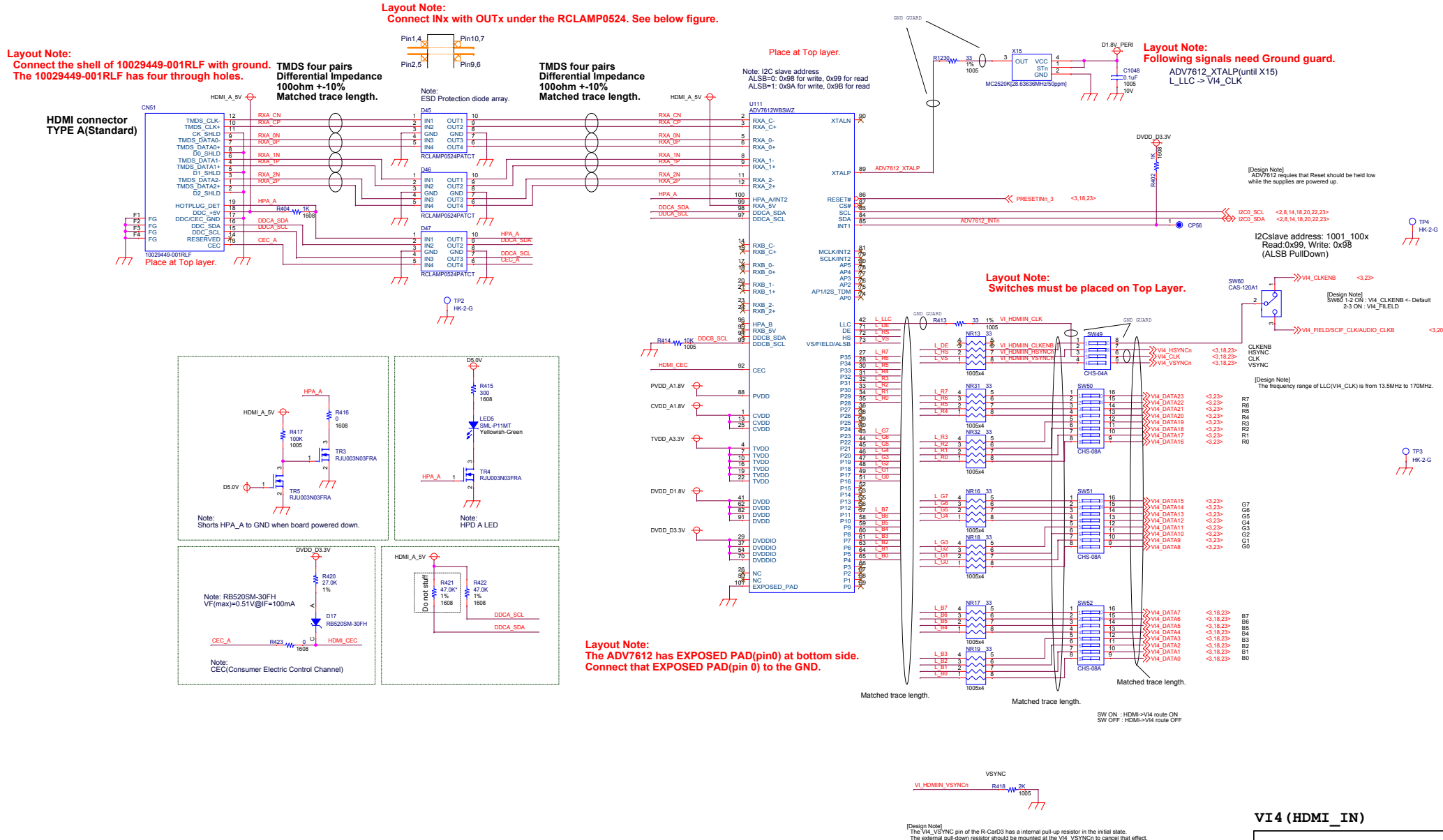

VI4(HDMI_IN)

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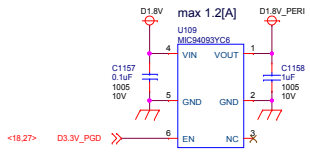
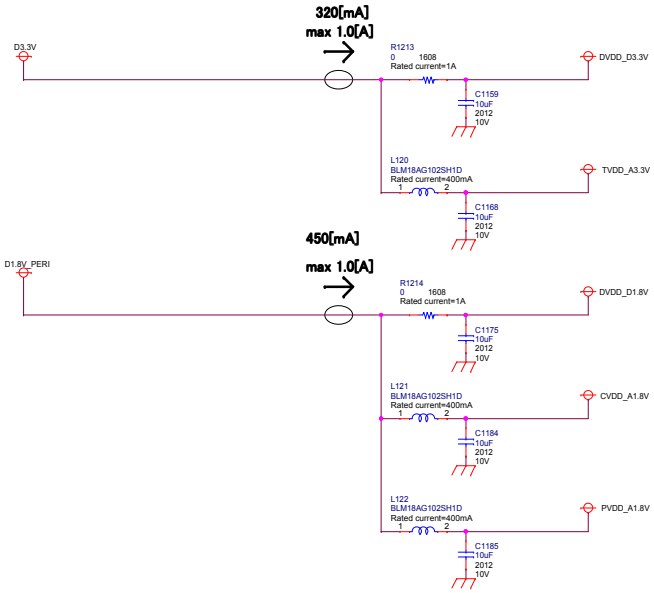
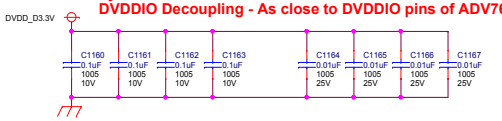
Load switch for ADV7612W

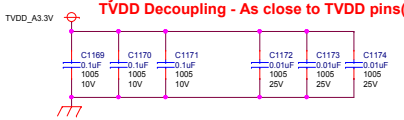




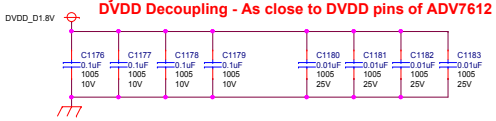
Layout Note:
DVDDIO Decoupling - As close to DVDDIO pins of ADV7612 as possible



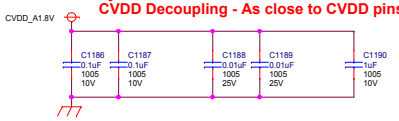
Layout Note:
TVDD Decoupling - As close to TVDD pins(pin4, pin7, pin10) of ADV7612 as possible



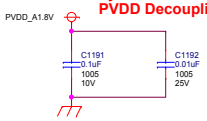
Layout Note:
DVDD Decoupling - As close to DVDD pins of ADV7612 as possible



Layout Note:
CVDD Decoupling - As close to CVDD pins(pin1, pin13) of ADV7612 as possible



Layout Note:
PVDD Decoupling - As close to PVDD pins of ADV7612 as possible



VI4 (HDMI_POWER)

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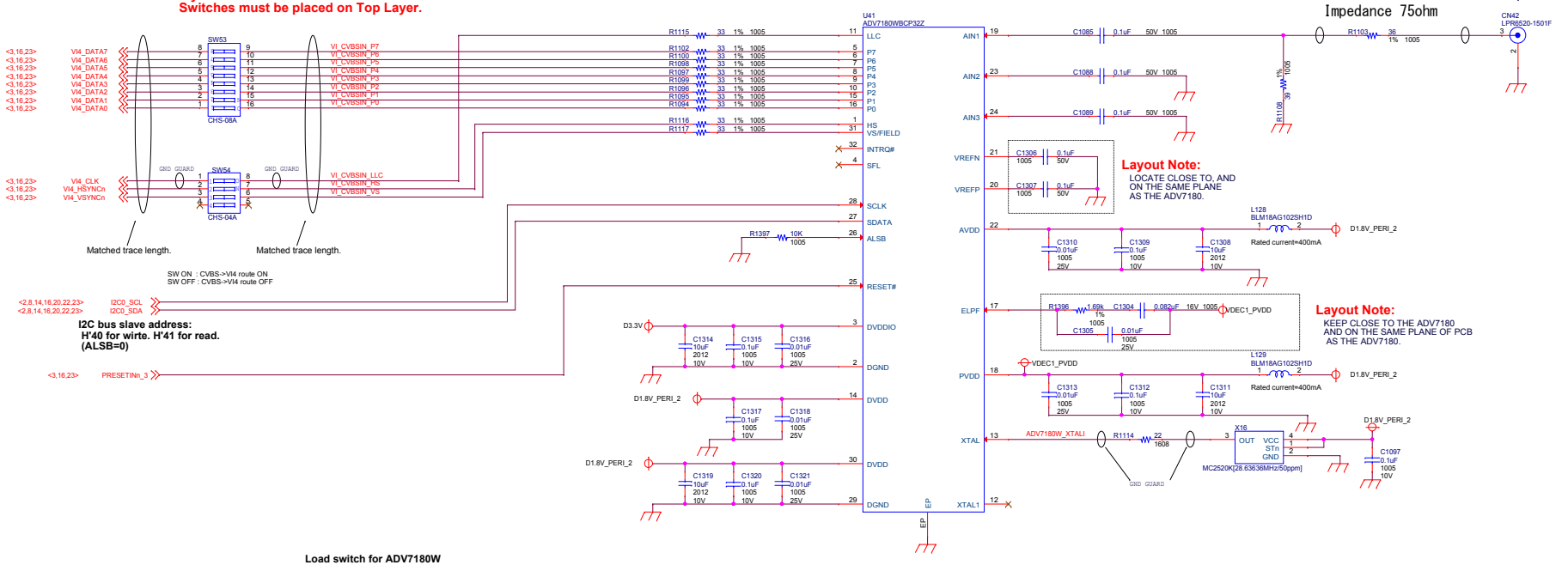
Layout Note:
Following signals need Ground guard.

ADV7180W_XTALI(until X16)
VI_CVBSIN_LLC -> VI4_CLK
CN42 -> U41 19pin

Layout Note:
Switches must be placed on Top Layer.

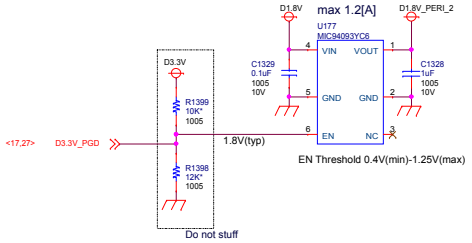


Layout Note:
LOCATE CLOSE TO, AND
ON THE SAME PLANE
AS THE ADV7180.

Layout Note:
KEEP CLOSE TO THE ADV7180
AND ON THE SAME PLANE OF PCB
AS THE ADV7180.

I2C bus slave address:
H'40 for wirte. H'41 for read.
(ALSB=0)

Load switch for ADV7180W



Layout Note:
ADV7180WBCP32Z has a exposed pad at bottom side.
Connect to GND(Digital GND).

VI4(CVBS_IN)

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Ethernet AVB GbPHY and PHY Connector

Layout Note:
As short as possible from junction of AVB0_xxx_VL to two Rxxx.

[R-CarD3 side] AVB0_xxx_VL — Rxxx — KSZ_xxx [KSZ9031 side]
Rxxx — EX_xxx [connector side]

Layout Note:
Matched Trace Length from R-CarD3 to KSZ9031.
(max 250Mbps/pin)

Group 1
AVB0_TXC_VL + KSZ_GTX_CLK
AVB0_TX_CTL_VL+KSZ_TX_EN
AVB0_TD[3:0]_VL + KSZ_TXD[3:0]
Group 2
AVB0_RXC_VL + KSZ_RX_CLK
AVB0_RX_CTL_VL + KSZ_RX_DV
AVB0_RD[3:0]_VL + KSZ_RXD[3:0]

<2> AVB0_TXC_VL	R641	0	1005	KSZ_GTX_CLK				
	R643	0*	1005	EX_GTX_CLK	<2> AVB0_RXC_VL	R642	1005 24.9 1%	KSZ_RX_CLK
<2> AVB0_TX_CTL_VL	R647	0	1005	KSZ_TX_EN		R644	0* 1005	EX_RX_CLK
	R651	0*	1005	EX_TX_EN	<2> AVB0_RX_CTL_VL	R648	1005 24.9 1%	KSZ_RX_DV
<2> AVB0_TD3_VL	R653	0	1005	KSZ_TXD3		R652	0* 1005	EX_RX_DV
	R658	0*	1005	EX_TXD3	<2> AVB0_RD3_VL	R654	1005 24.9 1%	KSZ_RXD3
<2> AVB0_TD2_VL	R659	0	1005	KSZ_TXD2		R657	0* 1005	EX_RXD3
	R662	0*	1005	EX_TXD2	<2> AVB0_RD2_VL	R660	1005 24.9 1%	KSZ_RXD2
<2> AVB0_TD1_VL	R664	0	1005	KSZ_TXD1		R663	0* 1005	EX_RXD2
	R666	0*	1005	EX_TXD1	<2> AVB0_RD1_VL	R665	1005 24.9 1%	KSZ_RXD1
<2> AVB0_TD0_VL	R668	0	1005	KSZ_TXD0		R667	0* 1005	EX_RXD1
	R670	0*	1005	EX_TXD0	<2> AVB0_RD0_VL	R669	1005 24.9 1%	KSZ_RXD0
	Do not stuff					R671	0* 1005	EX_RXD0
						Do not stuff		

Gigabit Ethernet Transceiver with RGMII Support

U78 KSZ9031RNXVA

KSZ_GTX_CLK	24	GTX_CLK	
KSZ_TX_EN	25	TX_EN	
KSZ_TXD3	22	TXD3	
KSZ_TXD2	21	TXD2	
KSZ_TXD1	20	TXD1	
KSZ_TXD0	19	TXD0	
KSZ_RX_CLK	35	RX_CLK/PHYAD2	
KSZ_RX_DV	33	RX_DV/CLK125_EN	
KSZ_RXD3	27	RXD3/MODE3	
KSZ_RXD2	28	RXD2/MODE2	
KSZ_RXD1	31	RXD1/MODE1	
KSZ_RXD0	32	RXD0/MODE0	
KSZ_MDC	36	MDC	
KSZ_MDIO	37	MDIO	
L_LED2/PHYAD1_VL	15	LED2/PHYAD1	
L_LED1/PHYAD0_VL	17	LED1/PME_N1/PHYAD0	
L_CLK125/LEDMD_VL	41	CLK125_NDO/LED_MODE	
KSZ_INTn	38	INT_N/PME_N2	
KSZ_RESETn	42	RESET_N	
KSZ_XO	45	XO	
KSZ_XI	46	XI	
	48	ISET	
	13	NC	
	43	NC	
	44	LDO_O	
	29	VSS	
	49	P_GND	

TP7 HK-2-G
DVDDH — R673 2K 1005
AVB0_MDC_VL, AVB0_MDIO_VL
X9 CX2016SA[25MHz/6pF/15ppm] KSZ_XO
C437 5pF 1005 50V — CL=6pF — C438 5pF 1005 50V
KSZ_XI
R320 12.1K 1% 1005

AVDDL_PLL: C754 0.01uF 1005 25V
AVDDH: C755 0.01uF 1005 25V, C756 0.01uF 1005 25V
AVDDL: C757 0.01uF 1005 25V, C758 0.01uF 1005 25V
DVDDH: C759 0.01uF 1005 25V, C760 0.01uF 1005 25V, C761 0.01uF 1005 25V
C762 0.1uF 1005 10V, C442 10uF 2012 16V
VDDQ25_AVB0 — R672 0
DVDDL: C764 0.01uF 1005 25V, C765 0.01uF 1005 25V, C766 0.01uF 1005 25V, C767 0.01uF 1005 25V, C768 0.01uF 1005 25V, C769 0.01uF 1005 25V
C770 0.1uF 1005 10V, C451 10uF 2012 16V
D1.2V — R675 0

Layout Note:
The KSZ9031RNX has Paddle Ground (pin49) at bottom side.
Connect that PAD(pin 49) to the GND.

RJ45 with integrated magnetics

CN22 0826-1G1T-23-F

TXRXP_A	2	TRD1P	LED1A
TXRXM_A	3	TRD1M	
		LED1K	
TXRXP_B	5	TRD2P	
TXRXM_B	6	TRD2M	
TXRXP_C	7	TRD3P	LED2A
TXRXM_C	8	TRD3M	
		LED2K	
TXRXP_D	10	TRD4P	
TXRXM_D	11	TRD4M	
AVDDL_PLL	44	TRCT1	
	1	TRCT2	
AVDDH	12	TRCT3	
AVDDH			
AVDDL	4	TRCT4	
AVDDL	9		
		SHIELD0	
		SHIELD1	

LED1A — R299 130 1005 — D3.3V
L_LED1 #[Activity[TX,RX]]
LED2A — R305 130 1005 — D3.3V
L_LED2 #[Link On]
C824 0.1uF 50V 1005, C825 0.1uF 50V 1005, C826 0.1uF 50V 1005, C827 0.1uF 50V 1005
SHIELD0 — R646 0 1005
SHIELD1 — R650 0 1005

Layout Note:
Following signals need Ground guard.
AVB0_TXCREFCLK_VL, CLK125/LEDMD_VL (125MHz)
AVB0_TXC_VL, KSZ_GTX_CLK, EX_GTX_CLK (125MHz)
AVB0_RXC_VL, KSZ_RX_CLK, EX_RX_CLK (125MHz)

Following pin has pull-down resistor at the initial state.
[2.5V-I/O]
AVB0_RX_CTL, AVB0_RXC, AVB0_RD[3:0]
AVB0_TX_CTL, AVB0_TXC, AVB0_TD[3:0]
AVB0_TXCREFCLK, AVB0_MAGIC, AVB0_PHY_INT, AVB0_LINK

Controls LEDs in the RJ45 connector

DVDDH — #[Link On] L_LED2 — R313 10K 1005 — L_LNK — TR6 RJU003N03FRA — TR8 RJU003N03FRA — L_LED2/PHYAD1_VL — R318 10K 1005
DVDDH — #[Activity[TX,RX]] L_LED1 — R314 10K 1005 — L_ACT — TR7 RJU003N03FRA — TR9 RJU003N03FRA — L_LED1/PHYAD0_VL — R319 10K 1005

LC filters for KSZ9031RNX

L96 BLM18AG102SH1D Rated current=400mA — D1.2V — AVDDL_PLL — VDDQ25_AVB0
C444 10uF 2012 16V, C763 0.1uF 1005 10V, C950 1000pF 1005 50V, C951 1uF 1005 10V
L97 BLM18AG102SH1D Rated current=400mA — D3.3V — AVDDH
C453 10uF 2012 16V, C771 0.1uF 1005 10V
L98 BLM18AG102SH1D Rated current=400mA — D1.2V — AVDDL
C454 10uF 2012 16V, C773 0.1uF 1005 10V

Local Regulator for KSZ9031RNX, PHY Connector

D3.3V, D1.2V
U37 ADP1707ARDZ-1.2-R7
IN, IN, EN, GND, OUT, OUT, SENSE, TRK, EP
C455 10uF 2012 16V, C456 10uF 2012 16V
max 1.0[A]
R1402 10K 1005 — R1401 4.7K 1005 — VDDQ25_AVB0

Layout Note:
The ADP1707 has EXPOSED PAD(pin9) at bottom side.
Connect that EXPOSED PAD(pin 9) to the GND.

DVDDH — R321 4.7K 1005 — <2> AVB0_PHY_INT_VL — AVB0_PHY_INT_VL

Strapping Options for KSZ9031RNX

DVDDH — R327 1K 1005, R329 1K 1005 — SW30 CHS-02A — L_LED2/PHYAD1_VL #[PHYAD1], L_LED1/PHYAD0_VL #[PHYAD0]
DVDDH — R752 2K 1005 AVB0_RX_CTL_VL #[CLK125_EN]
R753 2K 1005 AVB0_RD3_VL #[MODE3]
R754 2K 1005 AVB0_RD2_VL #[MODE2]
R755 2K 1005 AVB0_RD1_VL #[MODE1]
R756 2K 1005 AVB0_RD0_VL #[MODE0]
R757 2K 1005 AVB0_RXC_VL #[PHYAD2]

DVDDH — R676 2K 1005 — CP44 [Pin Function] GP5_18 — R323 0 1005 — <2> AVB0_MAGIC_VL
<3,11,20,22,23> PRESETOUTn — U35 HD74LV1G08A Level Shift(3.3V-->2.5V) — L_PHY_RESETn_VL
C774 0.1uF 1005 10V

[Design Note]
Remove zero ohm resistor avobe in case of using AVB0_MAGIC.

[Design Note]
HD74LV1G08A: VCC range=1.65V ~ 5.5V

Ethernet AVB PHY Connector

CN23 QSH-030-01-L-D-A

EX_RX_DV	2	IO	#[EtherAVB_MCLK]
EX_RXD3	4	IO	
EX_RXD2	6	IO	
#[AVB_RXD7]	8	IO	
EX_RXD1	10	IO	
EX_RXD0	12	IO	
EX_RX_CLK	14	IO	
#[AVB_RXD6]	16	IO	
#[AVB_RXD5]	18	IO	
#[AVB_RXD4]	20	IO	#[L_TESTM] EX_TX_EN
#[AVB_CRS]	22	IO	#[L_TESTC] EX_TXD3
#[AVB_RX_ERR]	24	IO	EX_TXD2
#[AVB_RX_COL]	26	IO	EX_TXD1
#[AVB_TX_CLK]	28	IO	#[SSI_WS0129] EX_TXD0
#[AVB_TX_ER]	32	IO	EX_GTX_CLK
#[AVB_TXD5]	34	IO	L_PHY_RESETn_VL
#[AVB_TXD4]	36	IO	AVB0_MDIO_VL
#[AVB_TXD7]	38	IO	AVB0_MDC_VL
#[AVB_TXD6]	40	IO	AVB0_PHY_INT_VL
#[AVB_GTXREFCLK]	42	IO	
	44	IO	
	46	IO	
	48	IO	
	50	IO	
	52	IO	
	54	IO	
	56	IO	
	58	IO	
	60	IO	
	1	IO	
	3	IO	
	5	IO	
	7	IO	
	9	IO	
	11	IO	
	13	IO	
	15	IO	
	17	IO	
	19	IO	
	21	IO	
	23	IO	
	25	IO	
	27	IO	
	29	IO	
	31	IO	
	33	IO	
	35	IO	
	37	IO	
	39	IO	
	41	IO	
	43	IO	
	45	IO	
	47	IO	
	49	IO	
	51	IO	
	53	IO	
	55	IO	
	57	IO	
	59	IO	
GND1	61	GND	
GND2	62	GND	
GND3	63	GND	
GND4	64	GND	

GR32, GR33, GR34

<2> I2C1_SDA, <2> I2C1_SCL
D3.3V, VDDQ25_AVB0, D1.2V

DVDDH — #[LED_MODE] — R325 10K 1005 — L_CLK125/LEDMD_VL
[Design Note]
LED_MODE==1, Single LED mode
LED_MODE==0, Tri-color dual-LED mode

<2> AVB0_TXCREFCLK_VL — f=125MHz — Do not stuff R788 22* 1608
2.5V X10 — MC2520K[125MHz/50ppm] — R334 22 1608 — VDDQ25_AVB0 — C457 0.01uF 1005 25V
Do not stuff R1373 22* 1608
VDDQ25_AVB0 — C1263 1005 0.01uF 25V — U173 SN74LVC1G04QDBVRQ1 — R1372 10K 1005 — VDDQ25_AVB0
R677 0 1005 — L_LNK
<2> AVB0_LINK_VL — R678 0* 1005 — L_ACT — Do not stuff

AVB_AVTP_PPS <2,23> MSIOF1_SCK/AVB_AVTP_PPS — CP58
AVB_AVTP_CAPTURE <2,23> MSIOF1_TXD/AVB_AVTP_CAPTURE — CP45
AVB_AVTP_MATCH <2,23> MSIOF1_RXD/AVB_AVTP_MATCH — CP46

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EtherAVB(GbPHY,PHY_CN) 19

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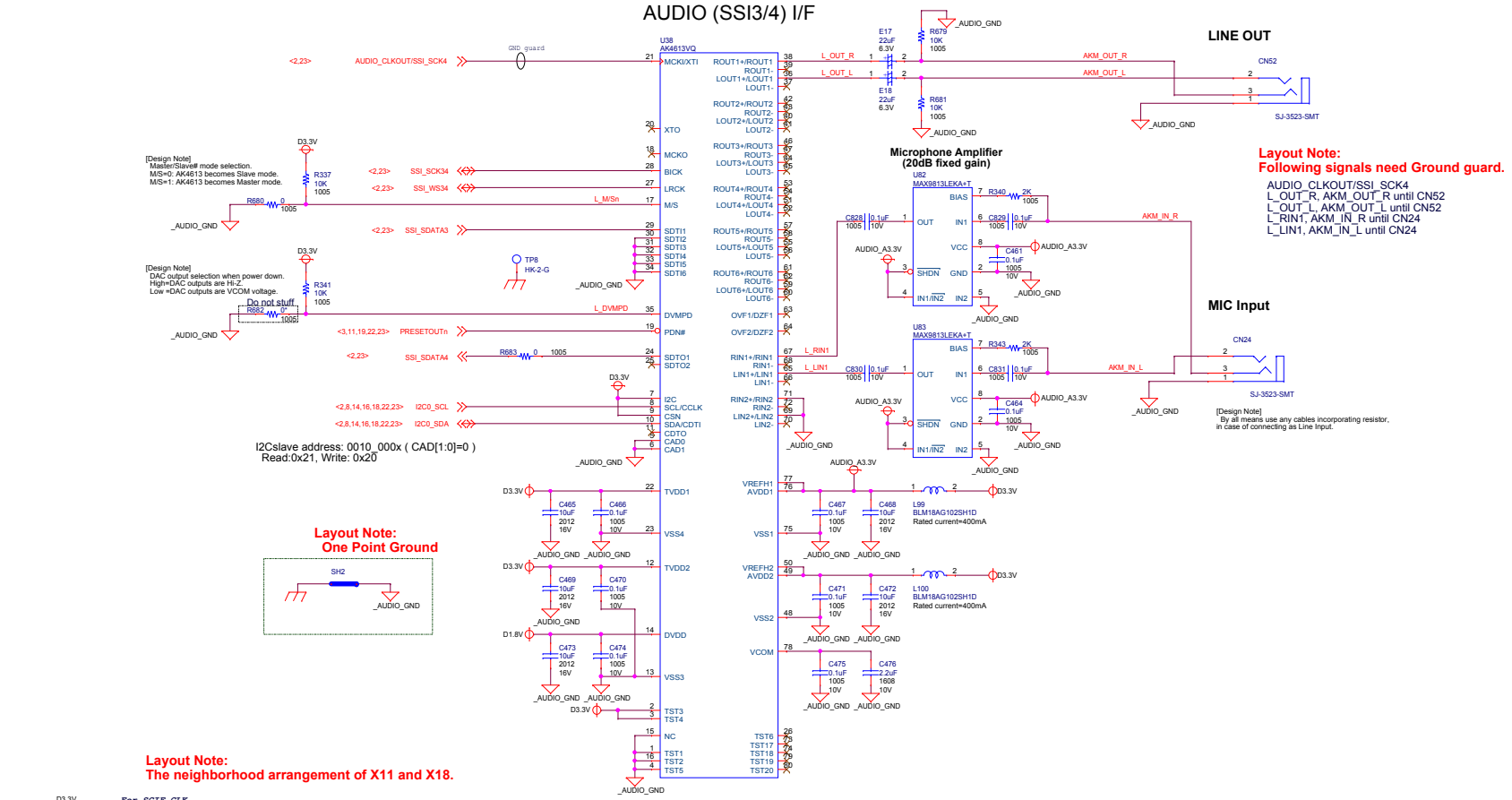
Preliminary



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AUDIO (AK4613VQ)

20

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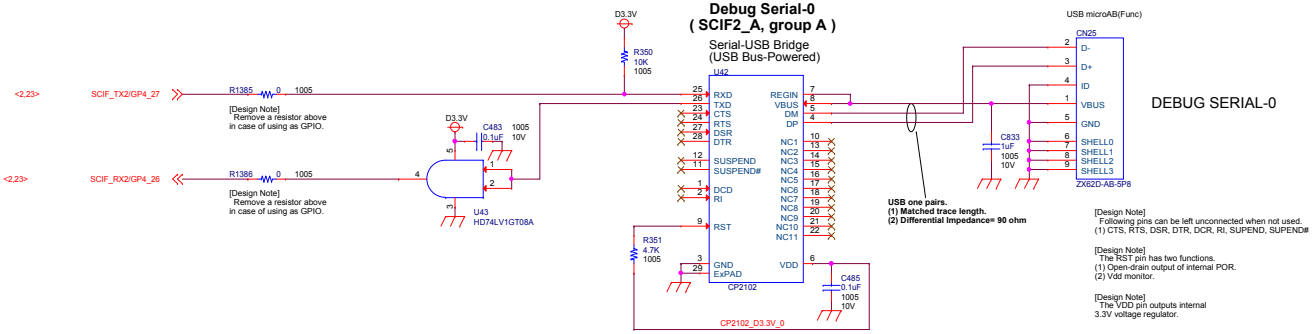
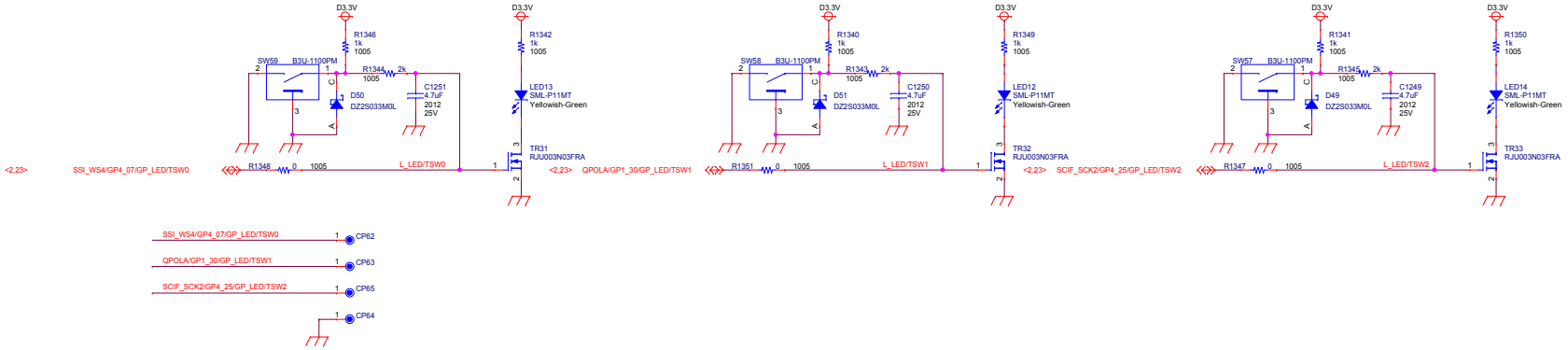


GPLED / Tact Switch



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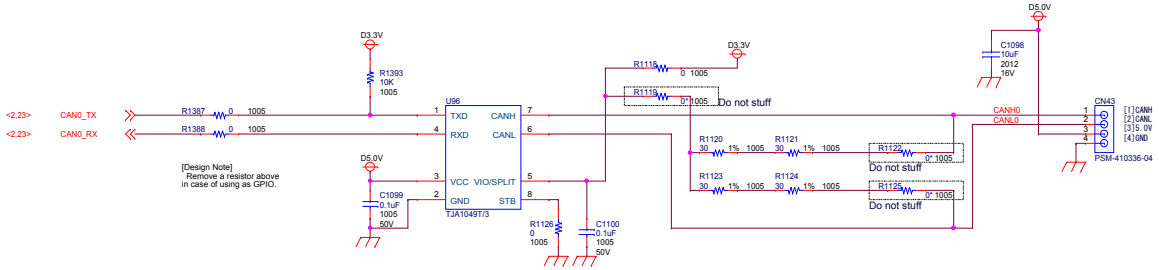
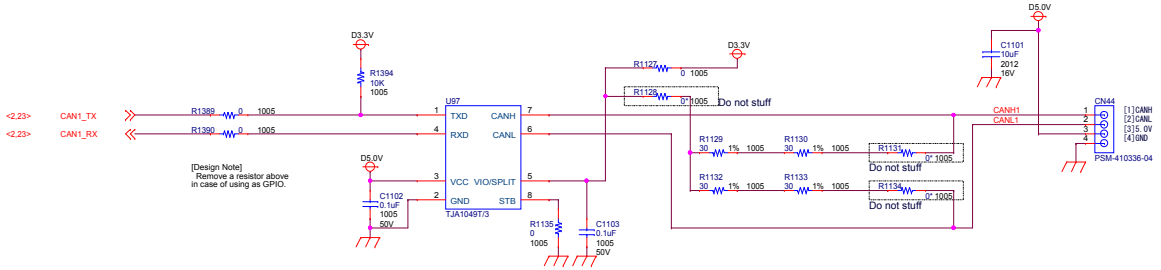
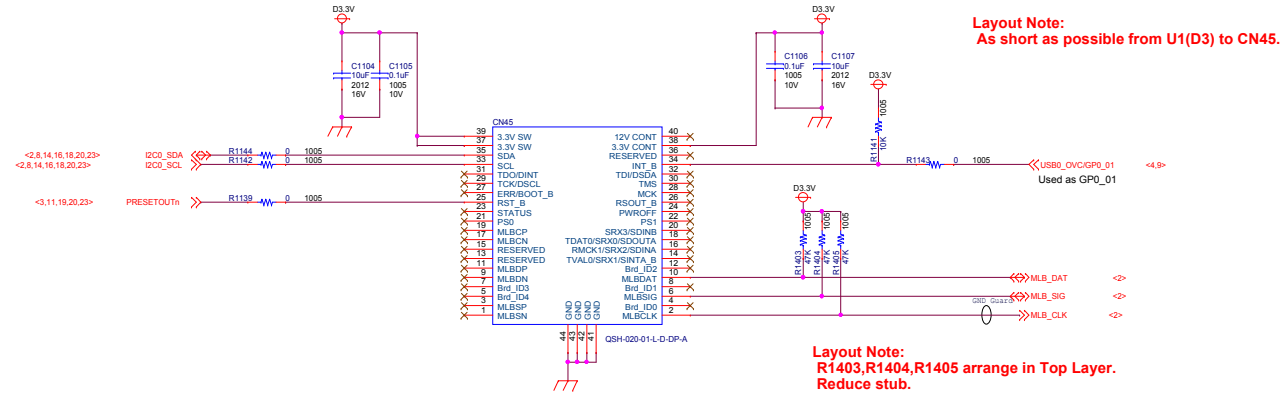
CAN0 I/F



CAN1 I/F



MOST CN



CAN/MOST_CN

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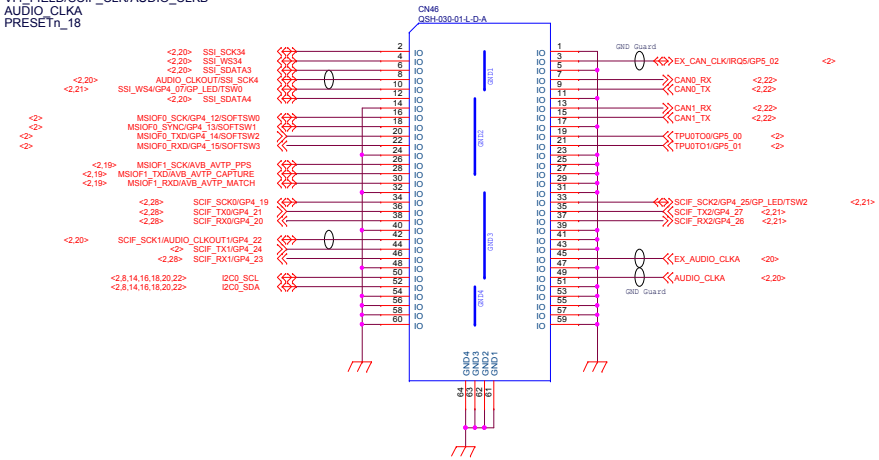
Layout Note:
Following signals need Ground guard.

EX_CAN_CLK/IRQ5/GP5_02,
EX_MMC_CLK_V,
VI4_CLK,DU_DOTCLKOUT0,
MLB_CLK,
EX_AUDIO_CLKA
EX_AUDIO_CLKB
AUDIO_CLKOUT/SSI_SCK4
SCIF_SCK1/AUDIO_CLKOUT1/GP4_22
VI4_FIELD/SCIF_CLK/AUDIO_CLKB
AUDIO_CLKA
PRESETn_18

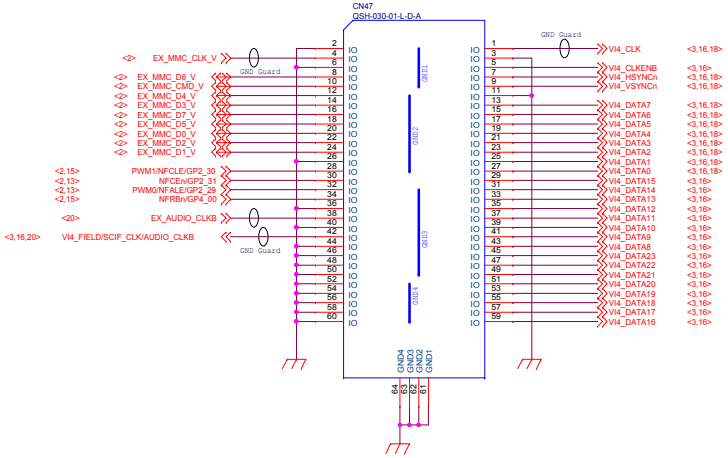
#[EXIO_A]

EXIO Connector A
(SSI,MSIOF,SCIF,I2C,CAN,TPU I/F)



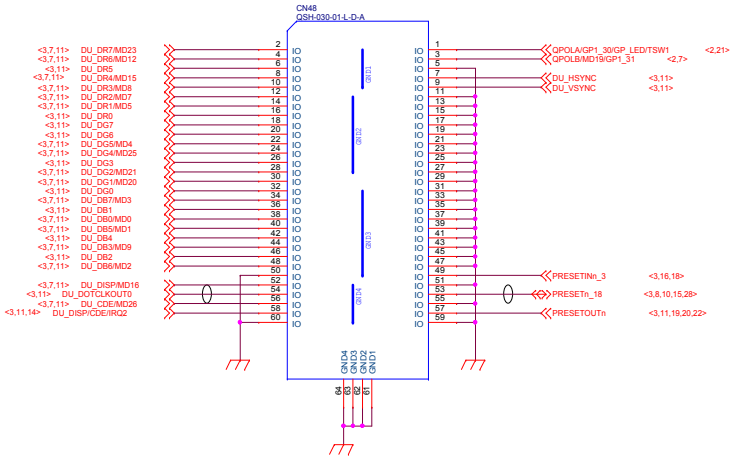
#[EXIO_B]

EXIO Connector B
(eMMC/NAND,VI4 I/F)



#[EXIO_C]

EXIO Connector C
(DU,TCON I/F)



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EXIO_CN

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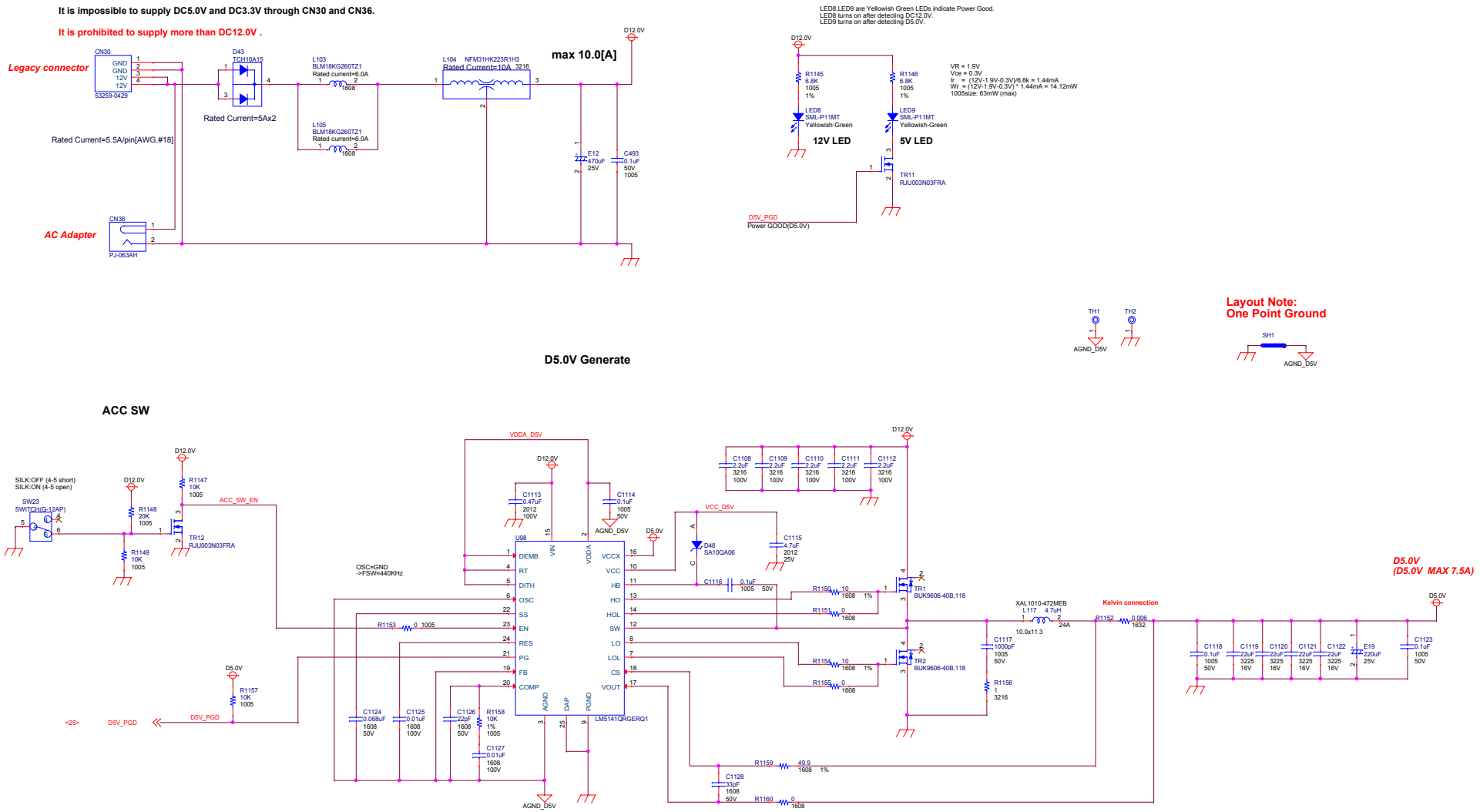

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Power IN/5V

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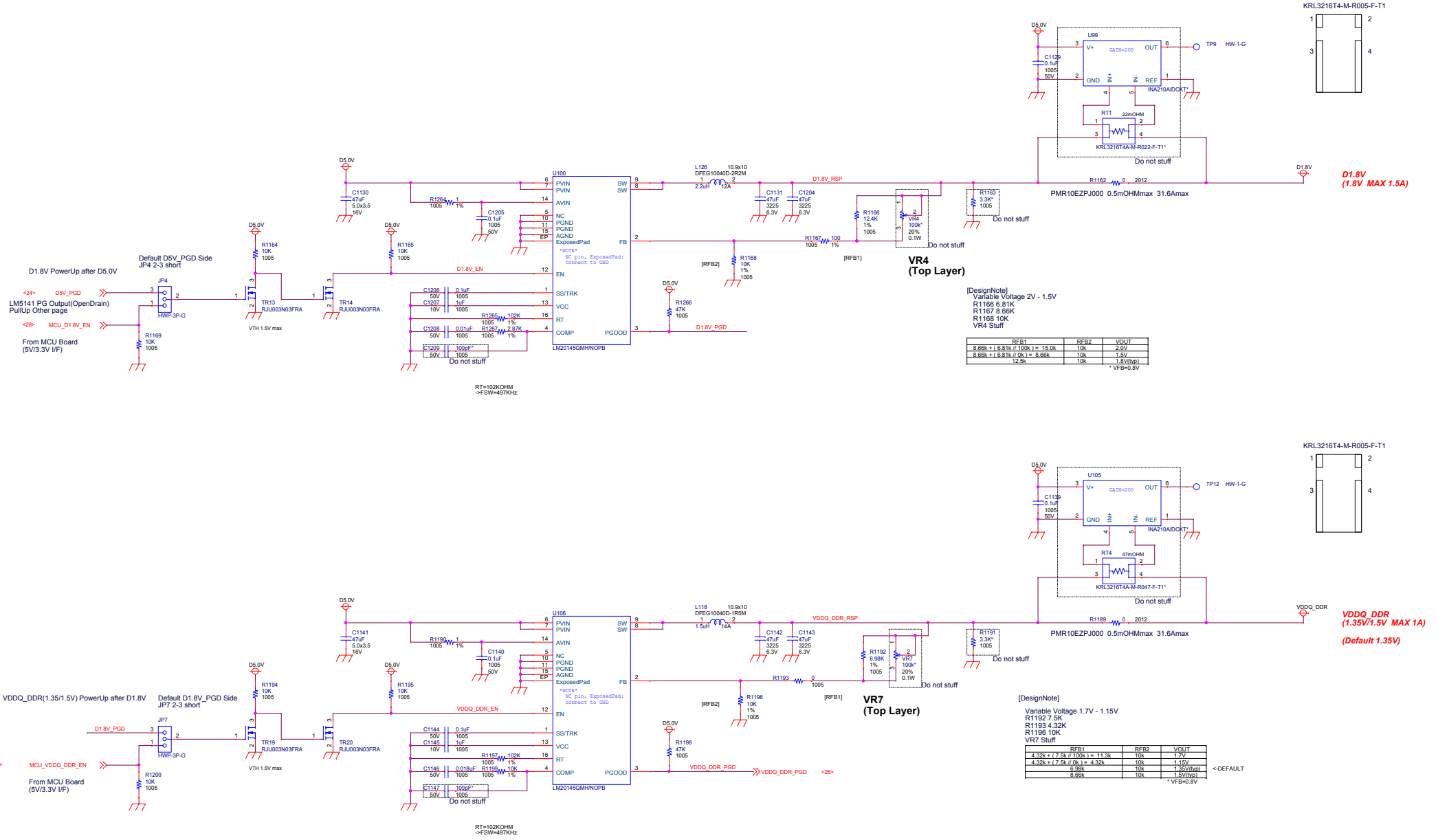

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POWER(1.8V/1.35V)

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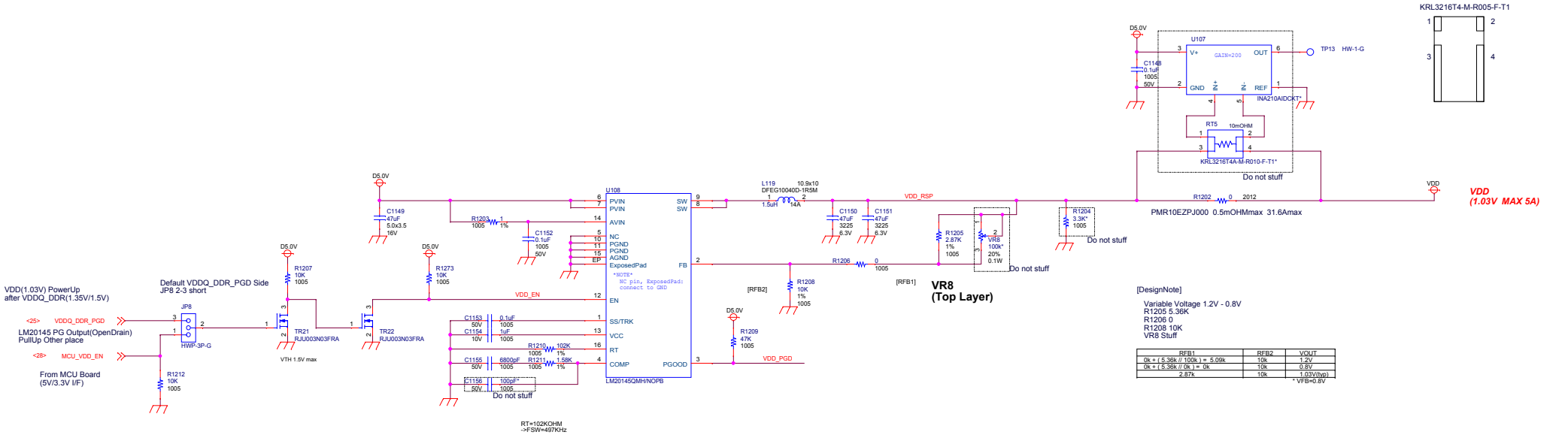

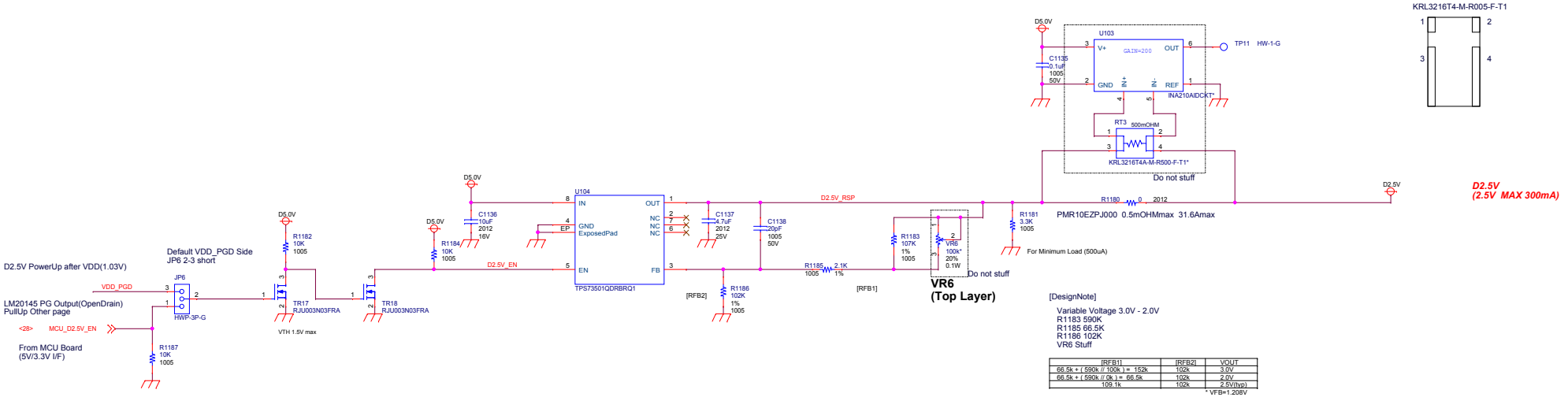

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POWER(1.03V/2.5V)

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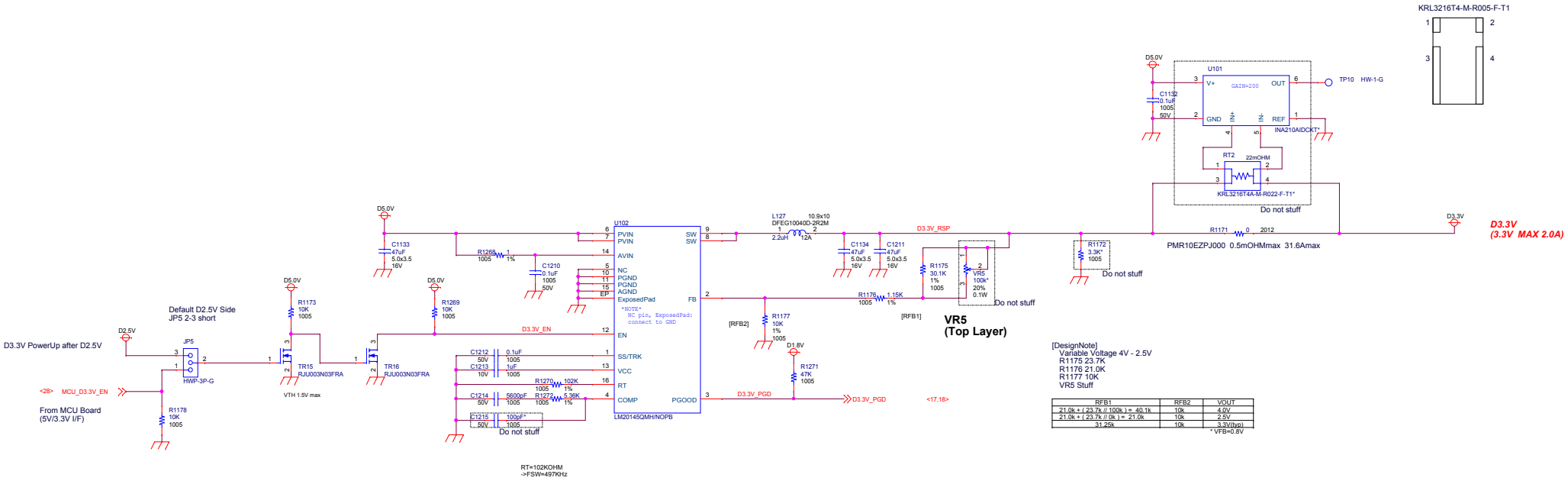

POWER(2.5V)

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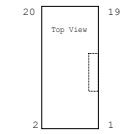
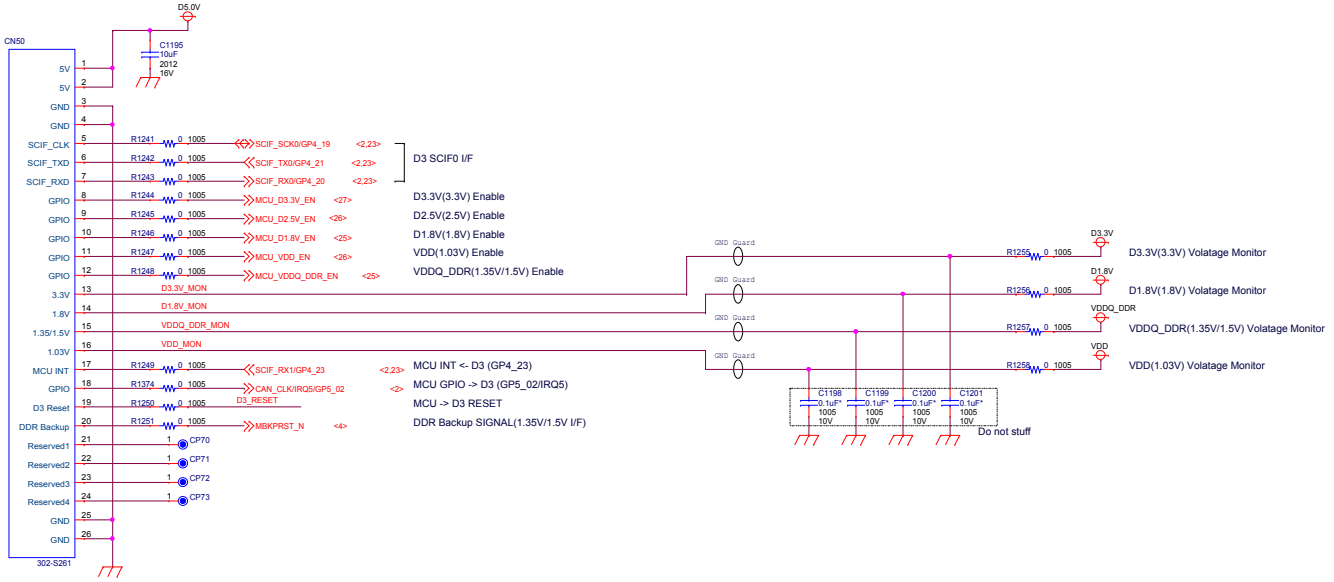
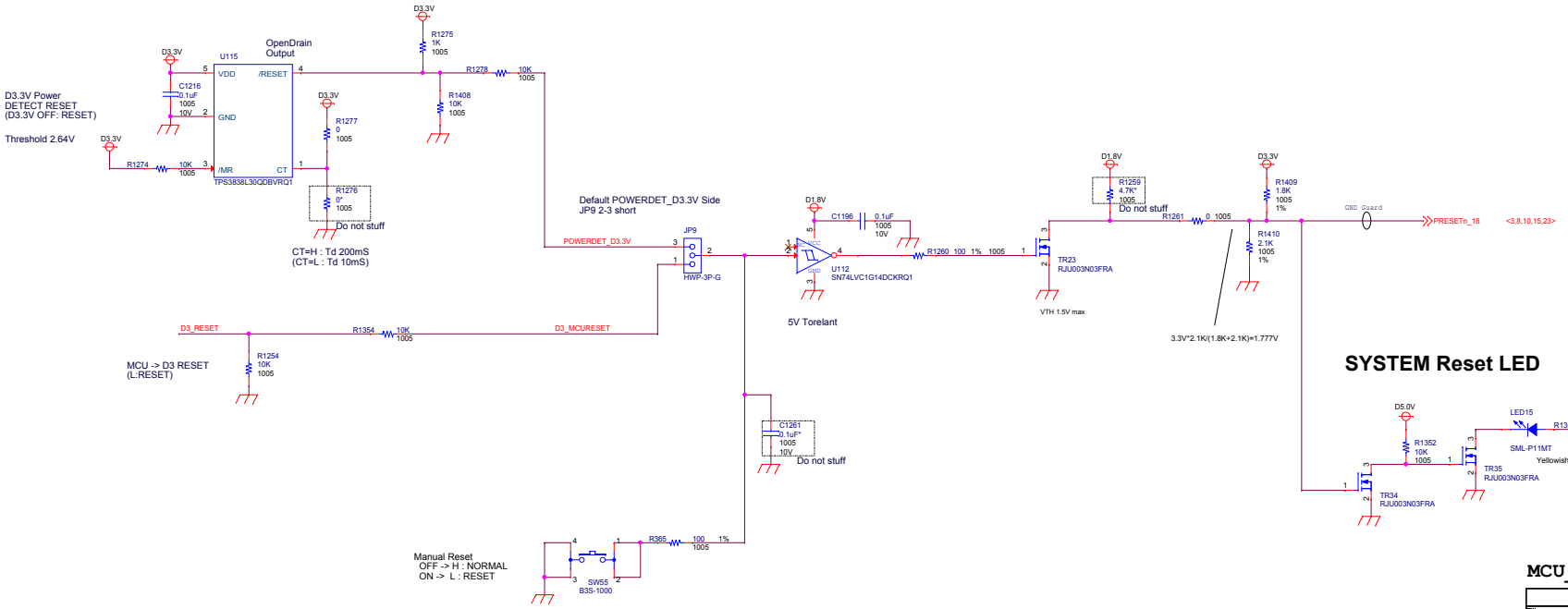
MCU BOARD CONNECTOR



Be carefull !!
See Pin Assignment.



RESET SIGNAL GENERATE



SYSTEM Reset LED

MCU_BOARD_CN/RST

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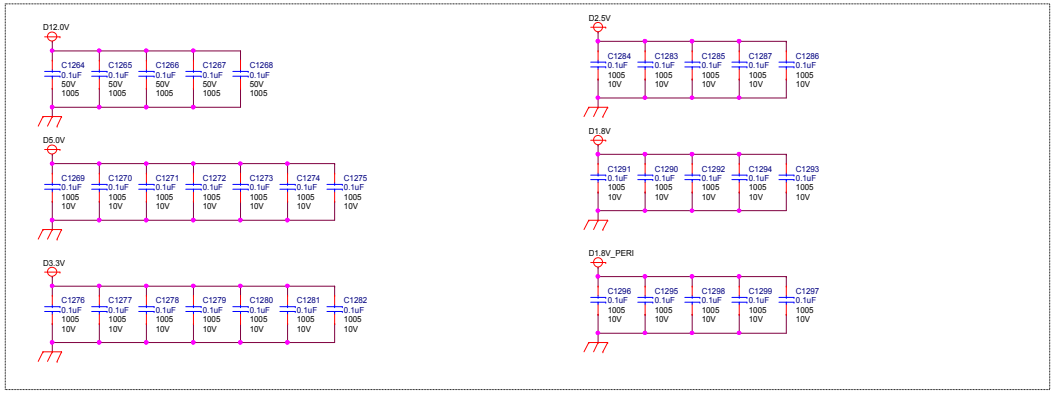
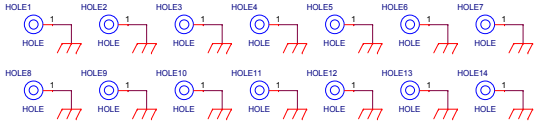
For EMI.



BOARD HOLE

BOARD hole is connected to GND.



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EMI_CAP

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