MiniPeriPeriCon

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July 11, 2016

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Core Additional Tasks

Scheduled for Phase 1 (8/M)

geert	R-Car H3 MSIOF Parent Clock Control Prototype
simon	R-Car M3-W Suspend-To-RAM Prototype
ulrich	R-Car M3-W SYS-DMAC Integration
laurent/kieran	*R-Car H3 Pin Function Controller Drive Strength of Non-I/O Pins Upstream Development (TBC)*

Core Additional Tasks

Planned for Phase 2 (9/M)

geert	Renesas-drivers Git Repository Maintenance
simon	R-Car M3-W Kexec Prototype
	...

Core Additional Tasks

Unplanned/not scheduled

- M3-W 64-bit memory support
- Prototype for DT fixup (first RFC sent)
- M3-W more suspend-to-ram
- M3-W PFC enhancements
- Migrate to CPG/MSSR
- Start adding dmas pointing to SYS-DMAC2 (needs secure firmware 2.8.0)
- ...

Discussion Topics

Dirk's Topics

- ESx.y
  1. API to access Product Register (PRR), used by drivers
  2. Fixup DT (change compatible value)
     - May need both? Latter is needed to e.g. change number of device instances
- Sharing clock definitions
- Sharing dtsi
  - Cfr. iMX6
  - SoC-specific: compatible value, core clocks, module clock (not CPG/MSSR), power area (although identical numbers per family)
  - Plain numbers in DT: IRQs, DMAs, module clocks (CPG/MSSR)

Discussion Topics

Additional Task Improvements

- Workflow improvements
- Increase transparency
- Priorities across groups
- ...